

Very Large Scale Integration (VLSI) Design

Course code :12EC54

Aug – Nov 2017

Unit II

CMOS PROCESSING TECHNOLOGY

Prepared by



Dr.Shylashree N

Associate Professor
Dept. Of ECE, RVCE
Bengaluru-59

OUTLINE

- CMOS Processing Technology
 - ▣ Crystal Growth
 - ▣ Photolithography
 - ▣ CMOS Technologies
 - ▣ Well & Channel formation – Epitaxy, Deposition, Implantation
 - ▣ Silicon dioxide – Oxidation
 - ▣ Isolation
 - ▣ Contacts & Metallization
 - ▣ Passivation
 - ▣ Metrology
- Lambda (λ) Design Rules
- Transistor Scaling

Prepared by Dr.Shylashree N

CMOS PROCESSING TECHNOLOGY

1. Crystal Growth

- ▣ Crystal growth method - Czochralski technique
- ▣ Wafer formation
- ▣ Wafer preparation
- ▣ Wafer characterization

Prepared by Dr.Shylashree N

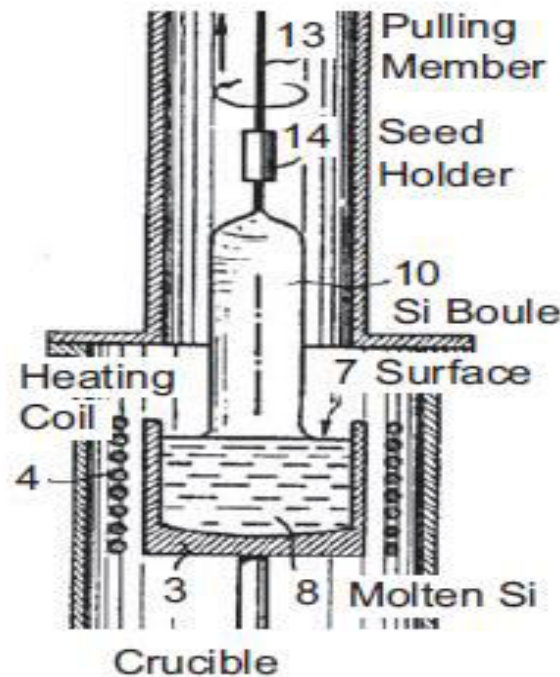
Wafer

- It is also called slice
- This is the basic physical unit and used in the processing
- It generally contains large number of ICs.
- Typically the wafer is circular and has diameters of 5 to 8 inches.

Crystal Growth Technique

The Wafers are cut from ingots of single crystal silicon that have been pulled from a crucible melt of pure molten silicon.

Prepared by Dr.Shylashree N



Czochralski Crystal Growth Apparatus

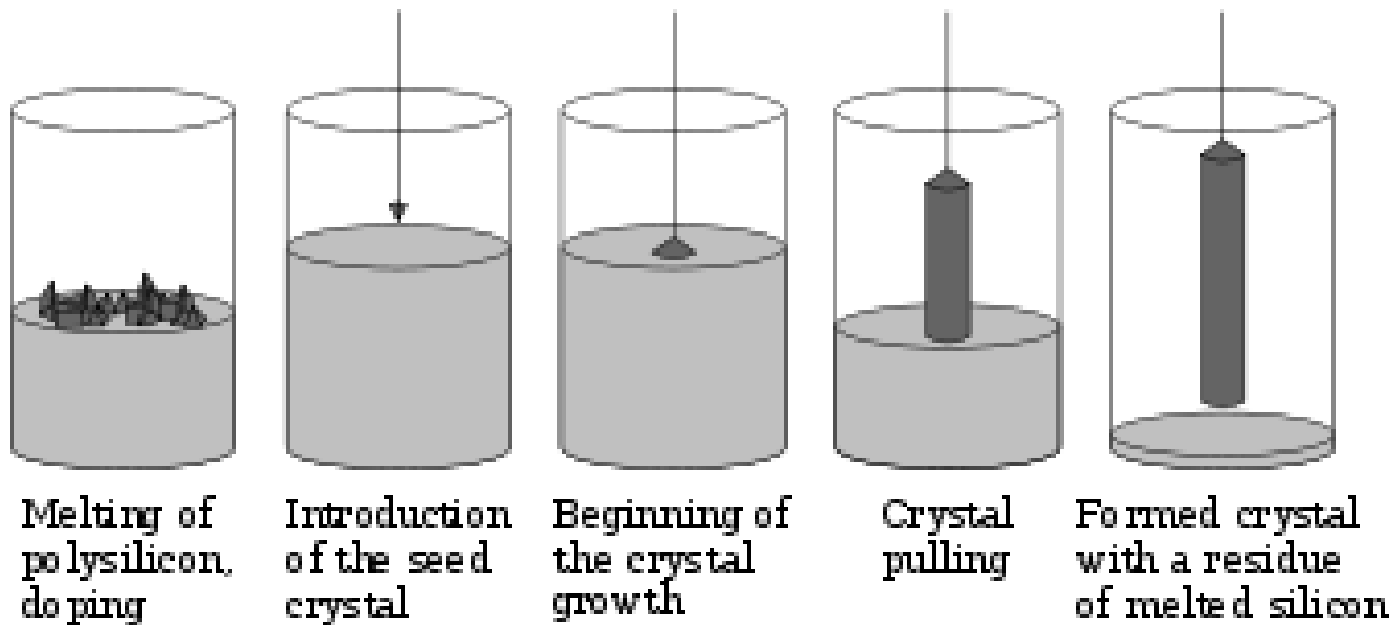
Wafer formation Contd..

- ❑ Controlled amounts of impurities are added to the melt to provide the crystal with the required electrical properties.
- ❑ A seed crystal is dipped in to the melt to initiate crystal growth.
- ❑ A graphite radiator heated by radio frequency induction surrounds the quartz crucible holding the melt and maintains the temperature a few degrees above the melting point of silicon

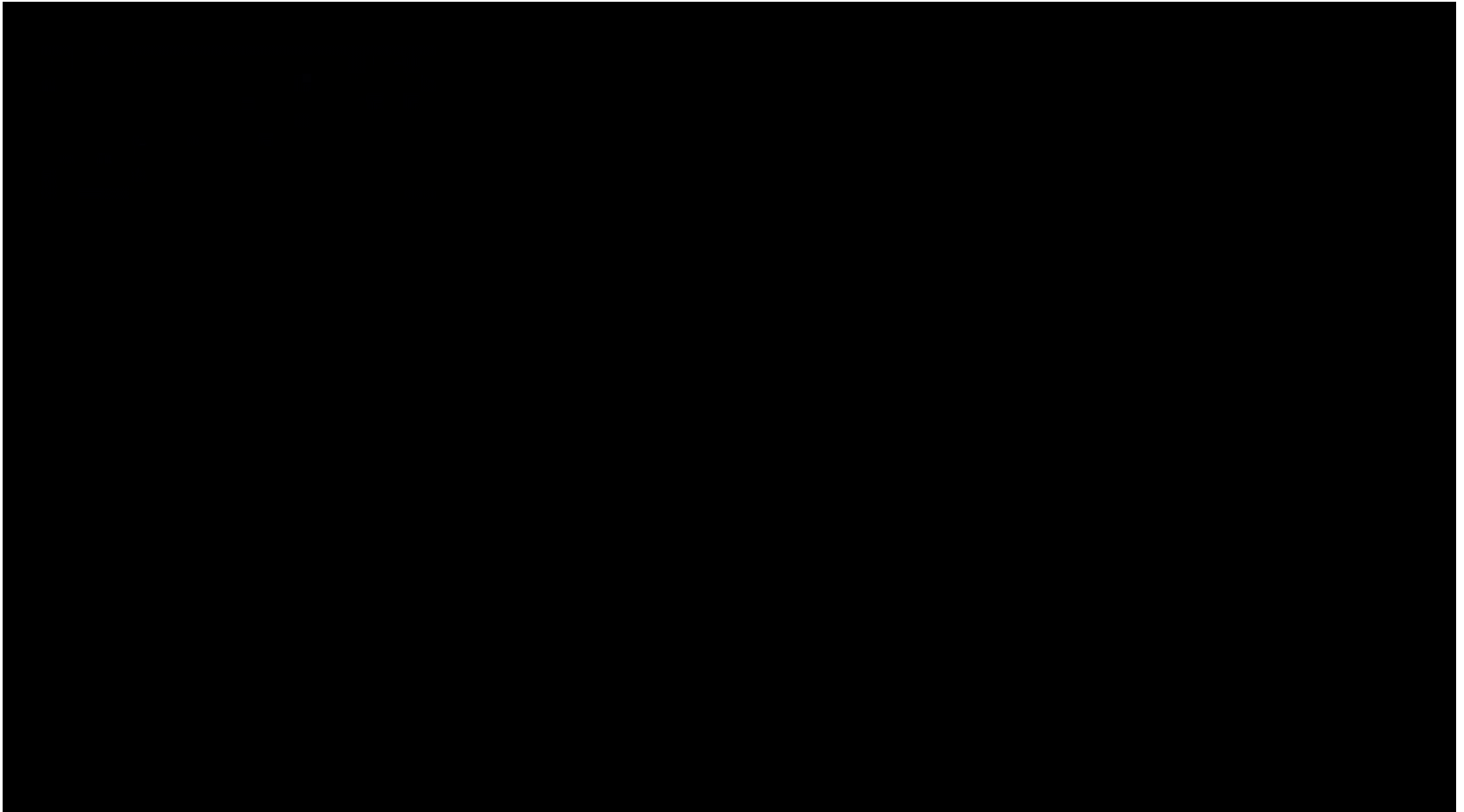
Wafer formation Contd..

- ❑ The atmosphere is typically helium to prevent the silicon from oxidizing.
- ❑ The seed is gradually with drawn vertically from the melt while simultaneously being rotated.
- ❑ The molten silicon attaches itself to the seed and recrystallizes as it is with drawn
- ❑ The seed withdrawal and rotation rates determine the diameter of the ingot.

CZ Process Steps



Wafer formation Video



<https://www.youtube.com/watch?v=AMgQ1-HdEIM> Prepared by Dr.Shylashree N

Ingot & Wafer

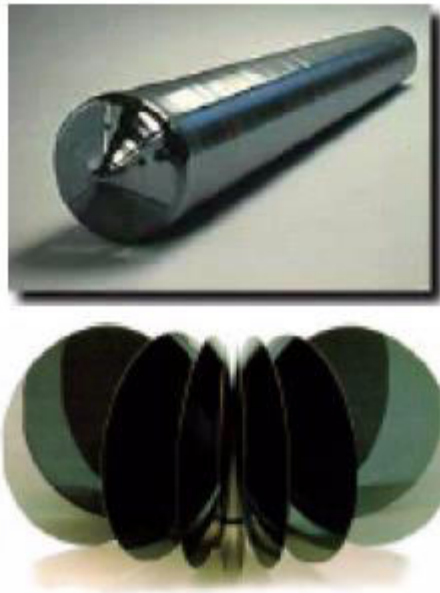


Figure 2.3 Single-crystal ingot and sliced wafers (from [Fullman99]).

CMOS PROCESSING TECHNOLOGY

2. Photolithography invented by Alphonse Poitevin (1855 incorporated light with lithography)

- ▣ Photo mask
- ▣ Photo resist
- ▣ Exposure techniques
- ▣ Resolution Enhancement Techniques
- ▣ Clean Room

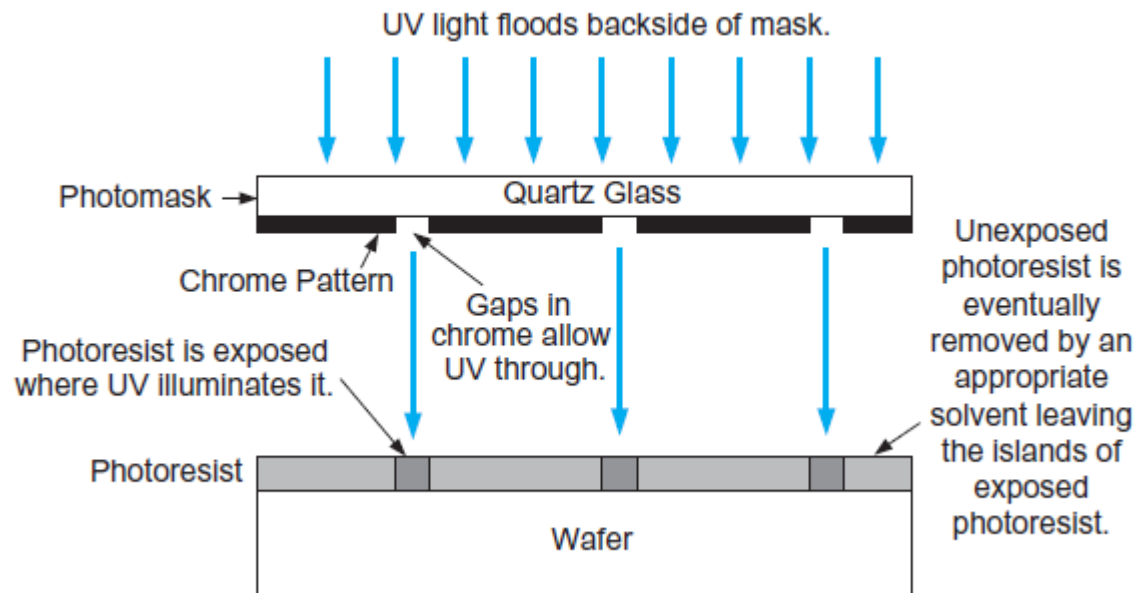
Prepared by Dr.Shylashree N

The patterning is achieved by a process called Photolithography, from the greek photo (light), Lithos (stone), and graphe (picture), which literally means “Carving pictures in stone using Light”

Components in Photolithography

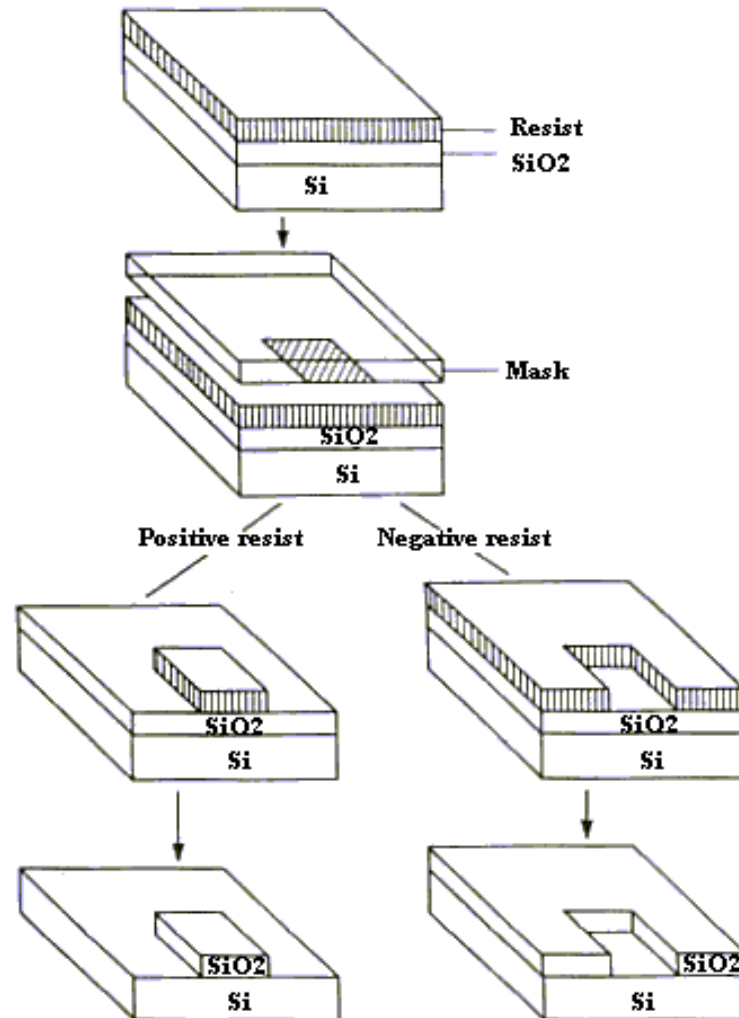
- ❑ Wafer
- ❑ Photoresist - Light sensitive material to define area
- ❑ Photomask / Reticle - Chromium covered quartz glass with desired pattern
- ❑ Lens
- ❑ UV Light Source is used to expose the photoresist.
- ❑ Developer Solution - selectively remove PR from the region where it was exposed

Photolithography



Photolithography is the technology to create a pattern on a silicon wafer using UV rays

Positive & Negative PR



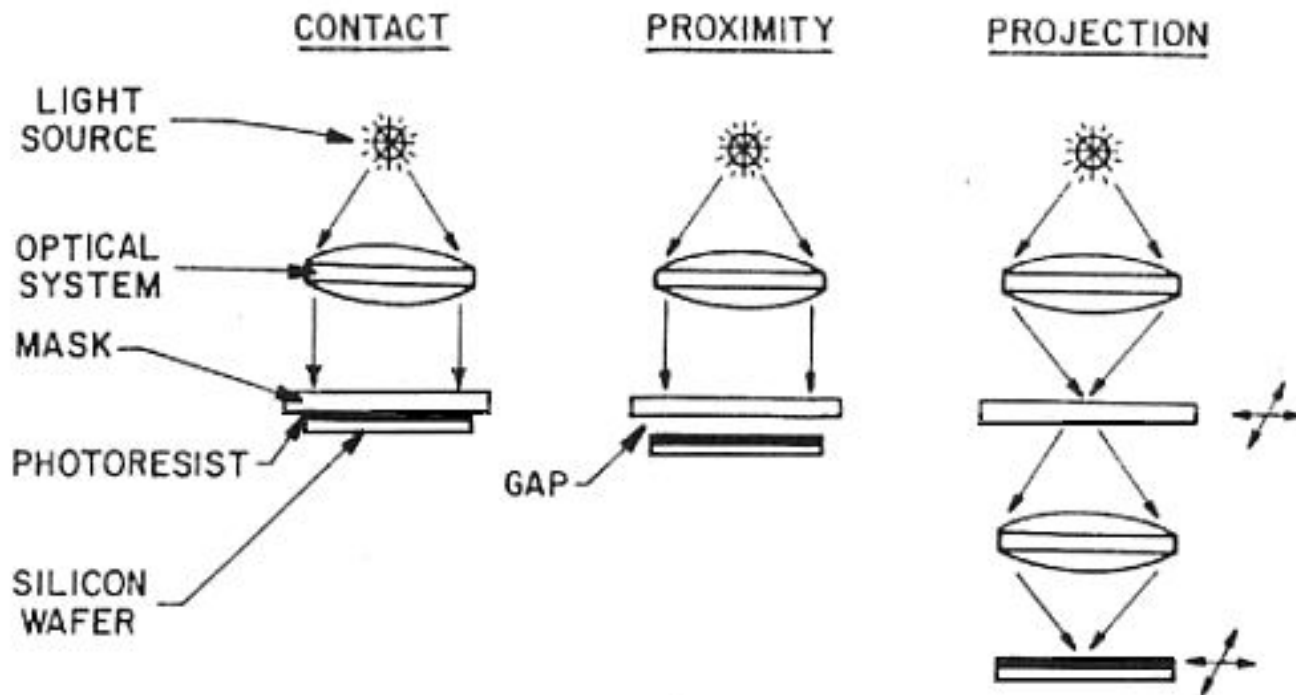
Prepared by
Dr.Shylashree N

Comparison of Positive & Negative PR

Positive PR	Negative PR
It is initially insoluble, and when exposed to UV becomes soluble	It is initially soluble, and when exposed to UV becomes insoluble
Provide higher resolution	Provide lower resolution
Less sensitive to light	More sensitive compared to positive PR
Pattern formed is same as mask	Pattern formed is inverse of mask

Prepared by Dr.Shylashree N

Exposure Techniques

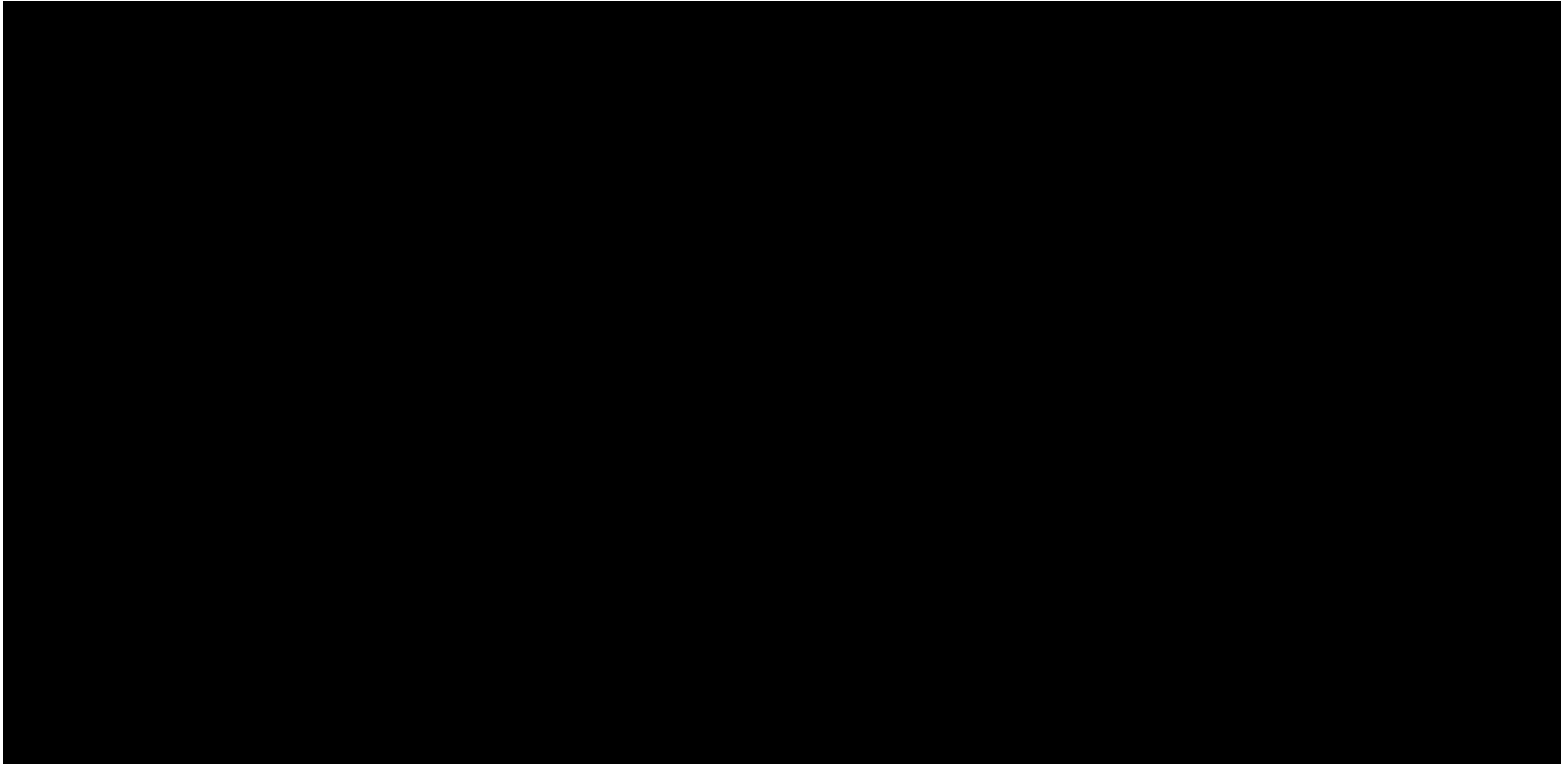


Prepared by Dr.Shylashree N

Comparison of different exposure techniques

Sl No	Shadow Printing		Projection Printing
	Contact	Proximity	
1	Wafer & Mask are in direct contact	Wafer & Mask are separated by a small distance	Wafer & Mask are separated by a larger distance
2	Reduced mask life & defects in the mask and resist	Gap eliminates defects but limitation on the minimum feature size that can be printed (increased diffraction effects)	Increased mask life

Photolithography video

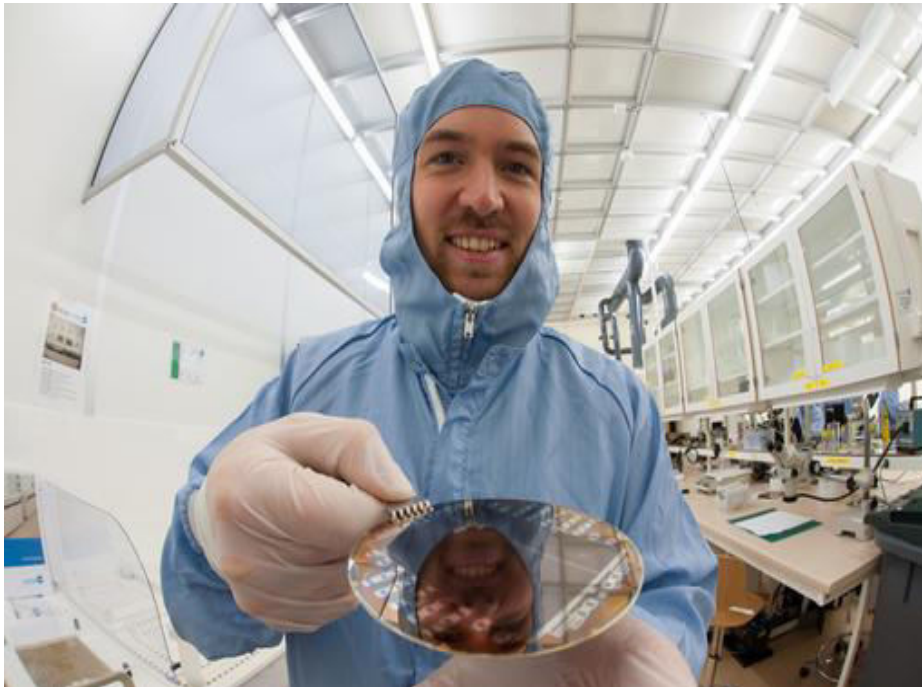


<https://www.youtube.com/watch?v=oBKhN4n-EGI>

Prepared by Dr.Shylashree N

Clean Room

- ❑ IC fabrication is done in a specially designed clean environment with a low level of environmental pollutants such as dust, airborne microbes, aerosol particles, and chemical vapours.



CMOS PROCESSING TECHNOLOGY

3. CMOS Technologies

- ▣ n well process
- ▣ p well process
- ▣ twin well process
- ▣ triple well process

n well process

Step1: Substrate

Primarily, start the process with a P-substrate.



Prepared by Dr.Shylashree N

n well process

Step2: Oxidation

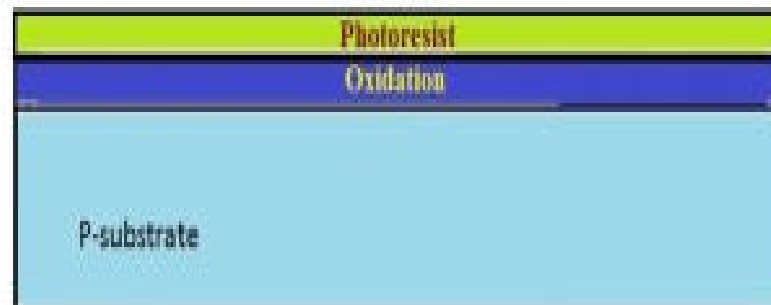
The oxidation process is done by using high-purity oxygen and hydrogen, which are exposed in an oxidation furnace approximately at 1000 degree centigrade.



n well process (...contd)

Step3: Photoresist

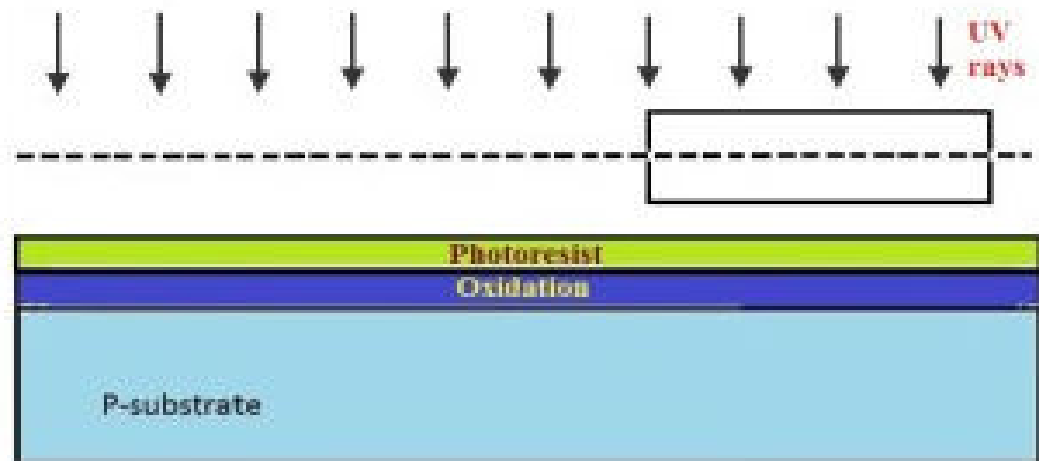
A light-sensitive polymer that softens whenever exposed to light is called as Photoresist layer. It is formed.



n well process (...contd)

Step4: Masking

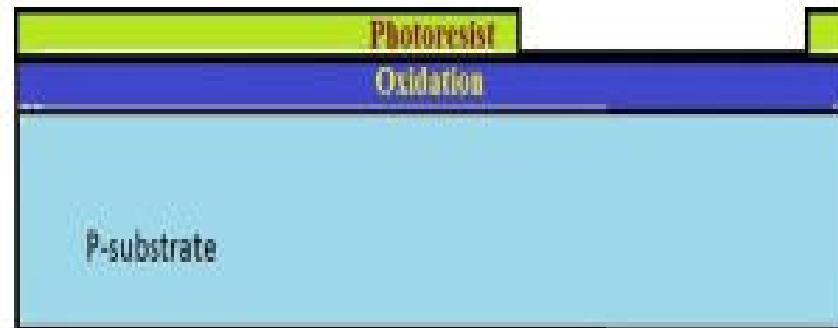
The photoresist is exposed to UV rays through the N-well mask



n well process (...contd)

Step5: Photoresist removal

A part of the photoresist layer is removed by treating the wafer with the basic or acidic solution.



n well process (...contd)

Step6: Removal of SiO₂ using acid etching

The SiO₂ oxidation layer is removed through the open area made by the removal of photoresist using hydrofluoric acid.



n well process (...contd)

Step7: Removal of photoresist

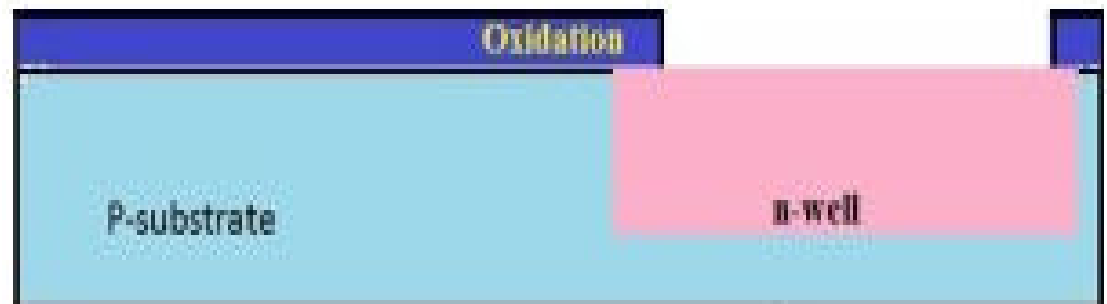
The entire photoresist layer is stripped off, as shown in the below figure.



n well process (...contd)

Step8: Formation of the N-well

By using ion implantation or diffusion process N-well is formed.

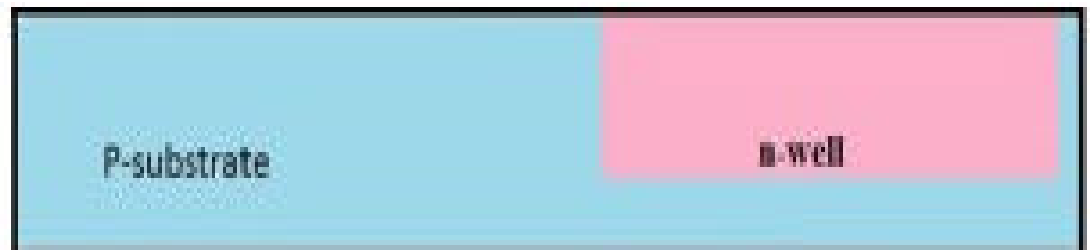


Prepared by Dr.Shylashree N

n well process

Step9: Removal of SiO₂

Using the hydrofluoric acid, the remaining SiO₂ is removed.



Prepared by Dr.Shylashree N

n well process

Step10: Deposition of polysilicon

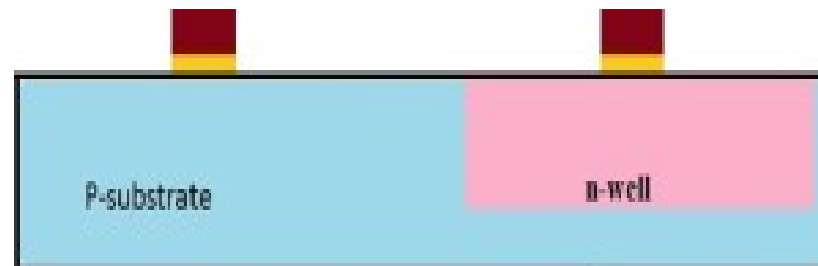
Chemical Vapor Deposition (CVD) process is used to deposit a very thin layer of gate oxide.



n well process

Step11: Removing the layer barring a small area for the Gates

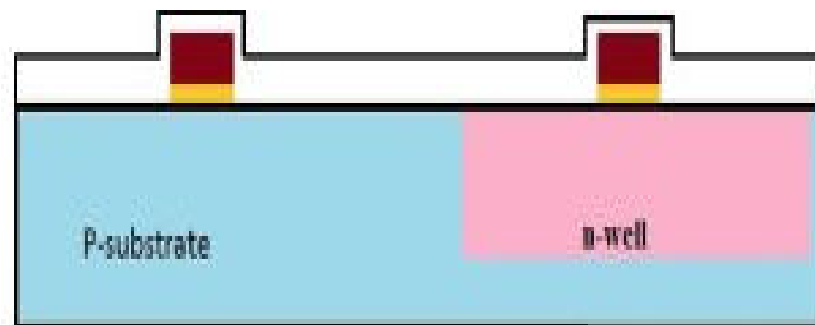
Except the two small regions required for forming the Gates of NMOS and PMOS, the remaining layer is stripped off.



n well process

Step12: Oxidation process

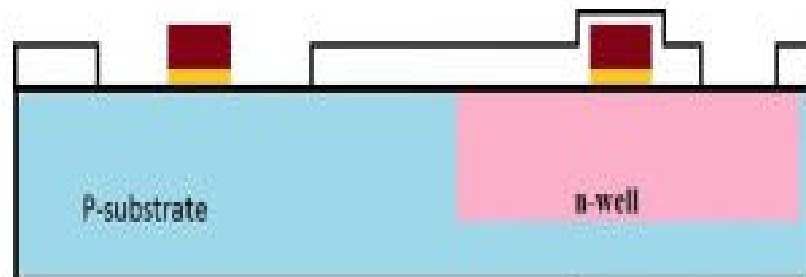
Next, an oxidation layer is formed on this layer with two small regions for the formation of the gate terminals of NMOS and PMOS.



n well process

Step13: Masking and N-diffusion

By using the masking process small gaps are made for the purpose of N-diffusion.



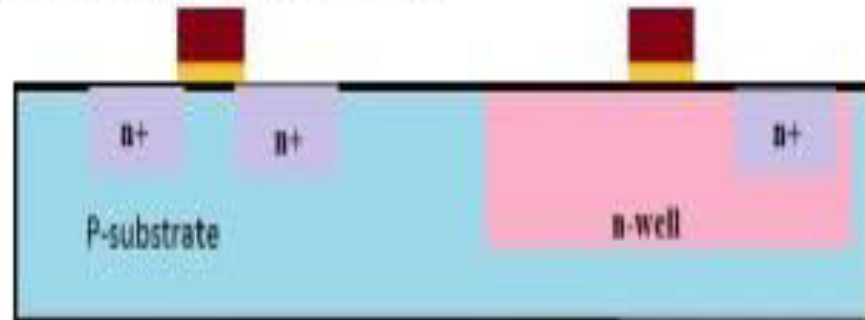
The n-type (n^+) dopants are diffused or ion implanted, and the three n^+ are formed for the formation of the terminals of NMOS.

Prepared by Dr.Shylashree N

n well process

Step14: Oxide stripping

The remaining oxidation layer is stripped off.



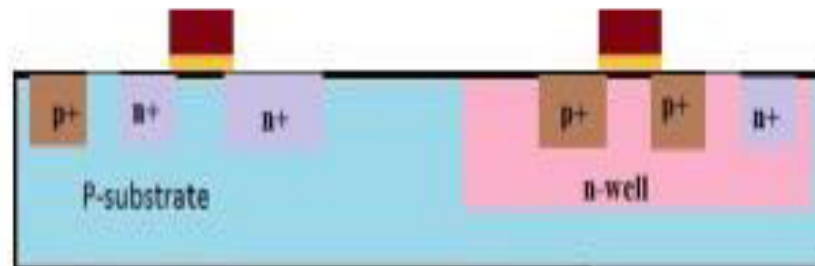
Prepared by Dr.Shylashree N

n well process

Step15: P-diffusion

Similar to the above N-diffusion process, the P-diffusion regions are diffused to form the terminals of the PMOS.

Prepared by Dr.Shylashree N

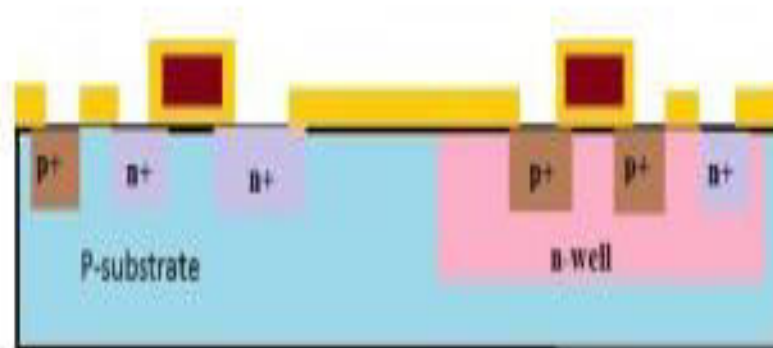


n well process

Step16: Thick field oxide

Prepared by Dr.Shylashree N

A thick-field oxide is formed in all regions except the terminals of the PMOS and NMOS.

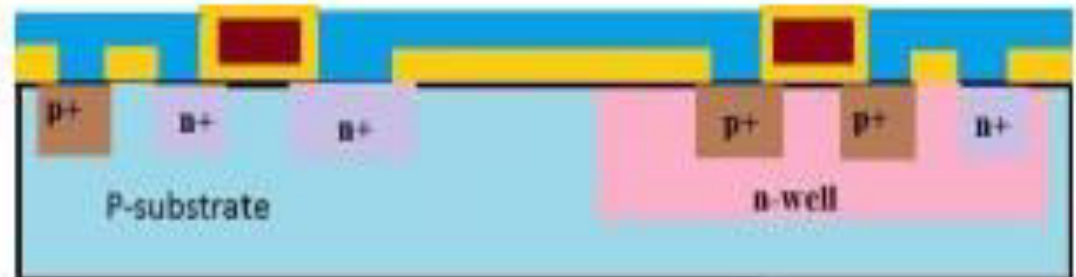


n well process

Step17: Metallization

Prepared by Dr.Shylashree N

Aluminum is sputtered on the whole wafer.

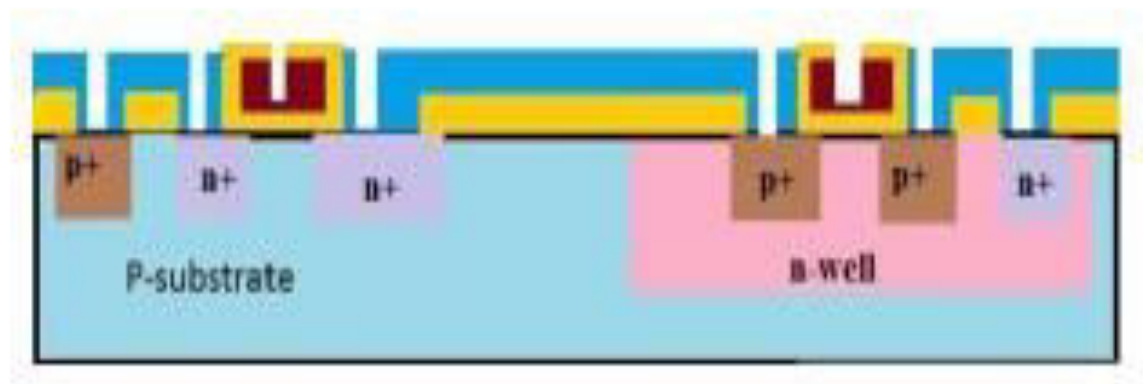


n well process

Step18: Removal of excess metal

Prepared by Dr.Shylashree N

The excess metal is removed from the wafer layer.

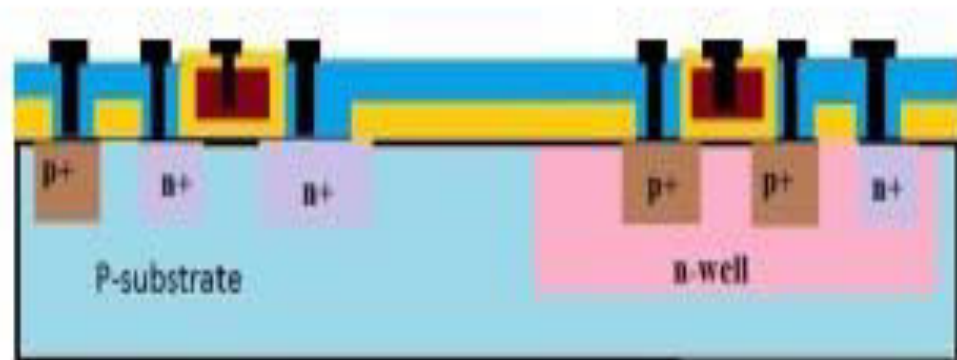


n well process

Step19: Terminals

Prepared by Dr.Shylashree N

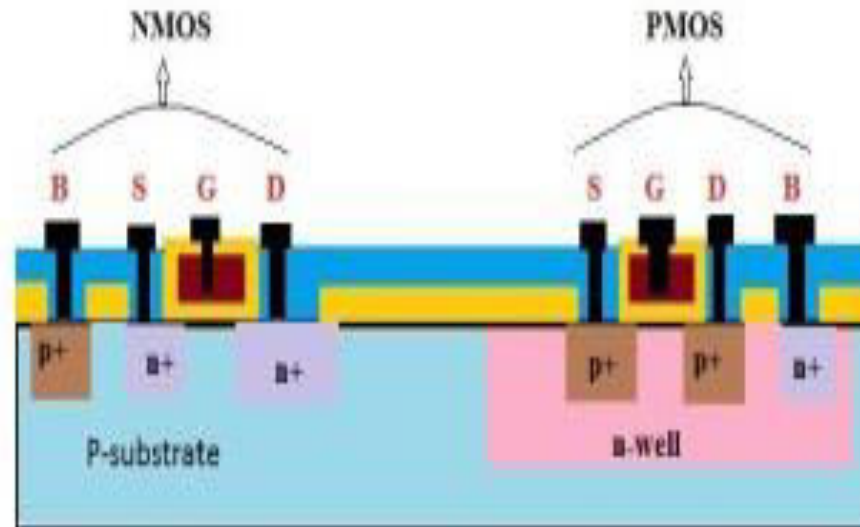
The terminals of the PMOS and NMOS are made from respective gaps.



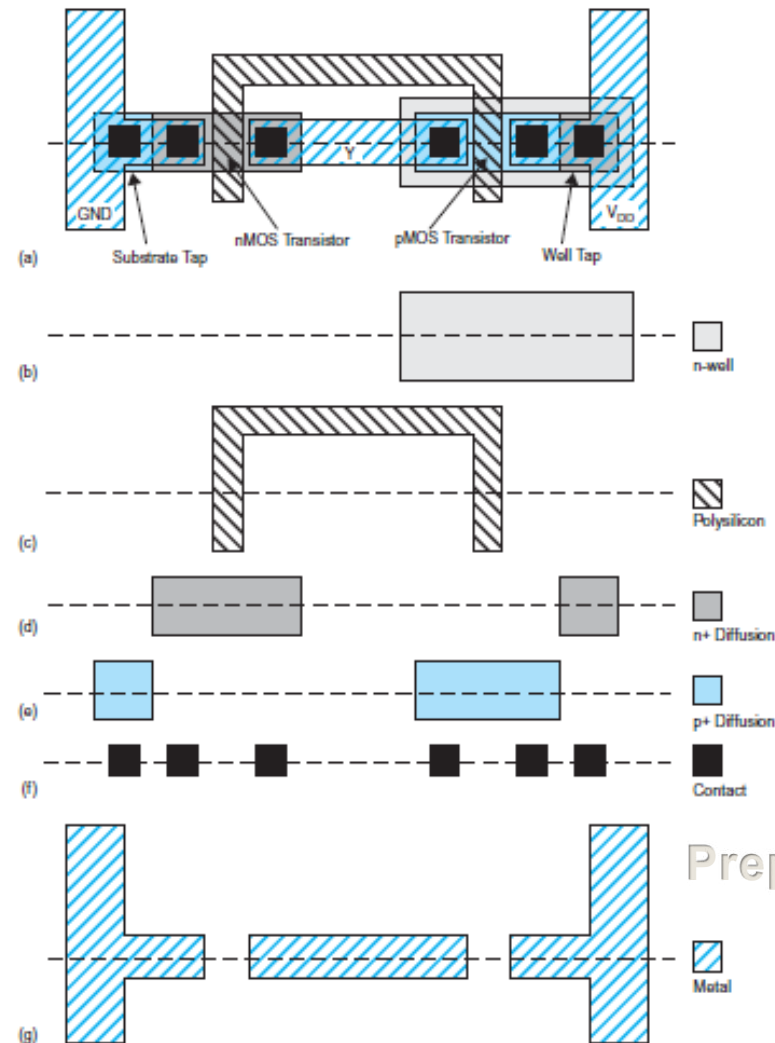
n well process

Step20: Assigning the names of the terminals of the NMOS and PMOS

Prepared by Dr.Shylashree N



Inverter Mask Set

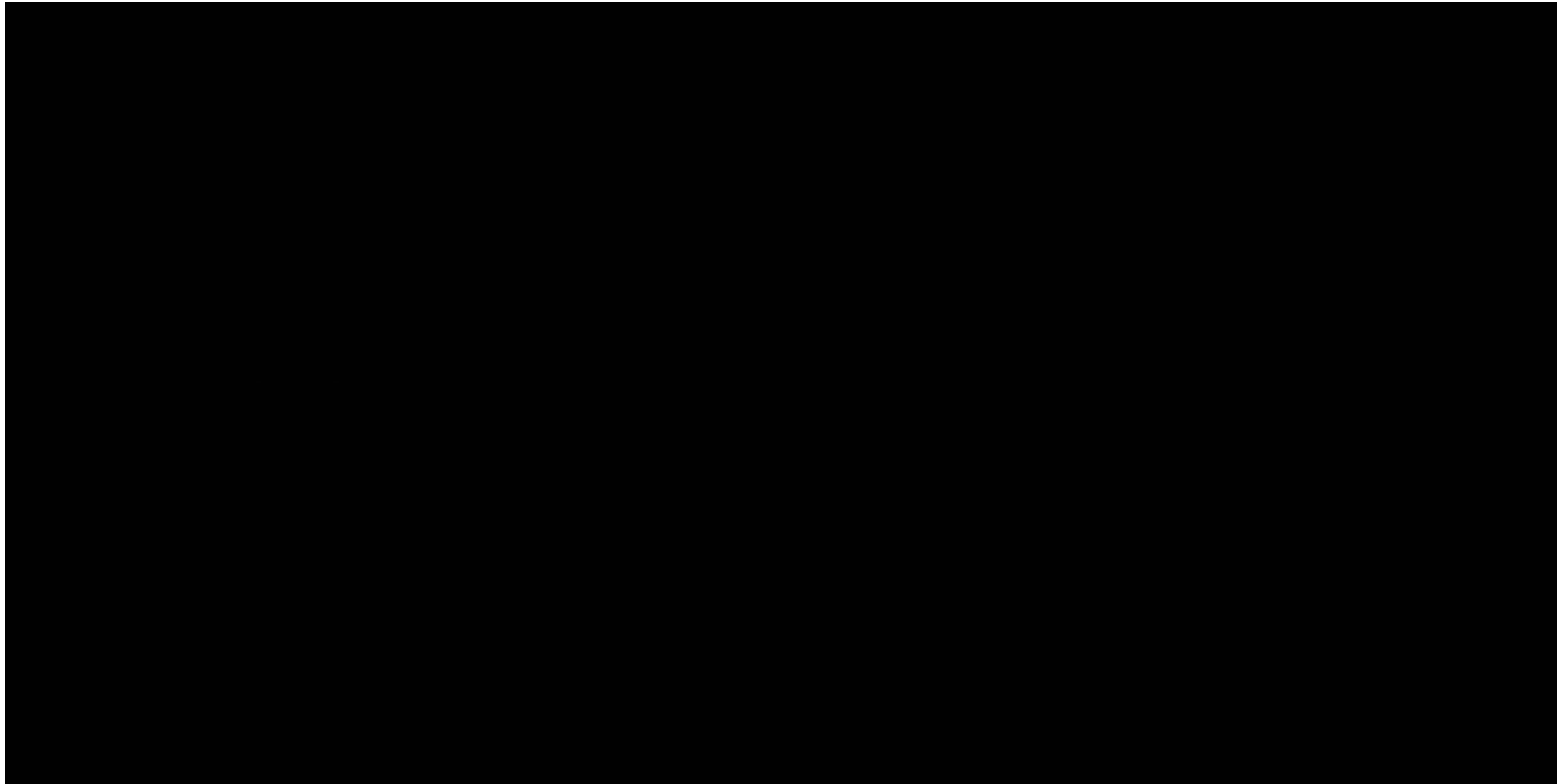


Prepared by Dr.Shylashree N

pwell process

- Among all the fabrication processes of the CMOS, N-well process is mostly used for the fabrication of the CMOS.
- p-well process is almost similar to the N-well. But the only difference in p-well process is that it consists of a main N-substrate and, thus, p-wells itself acts as substrate for the N-devices.

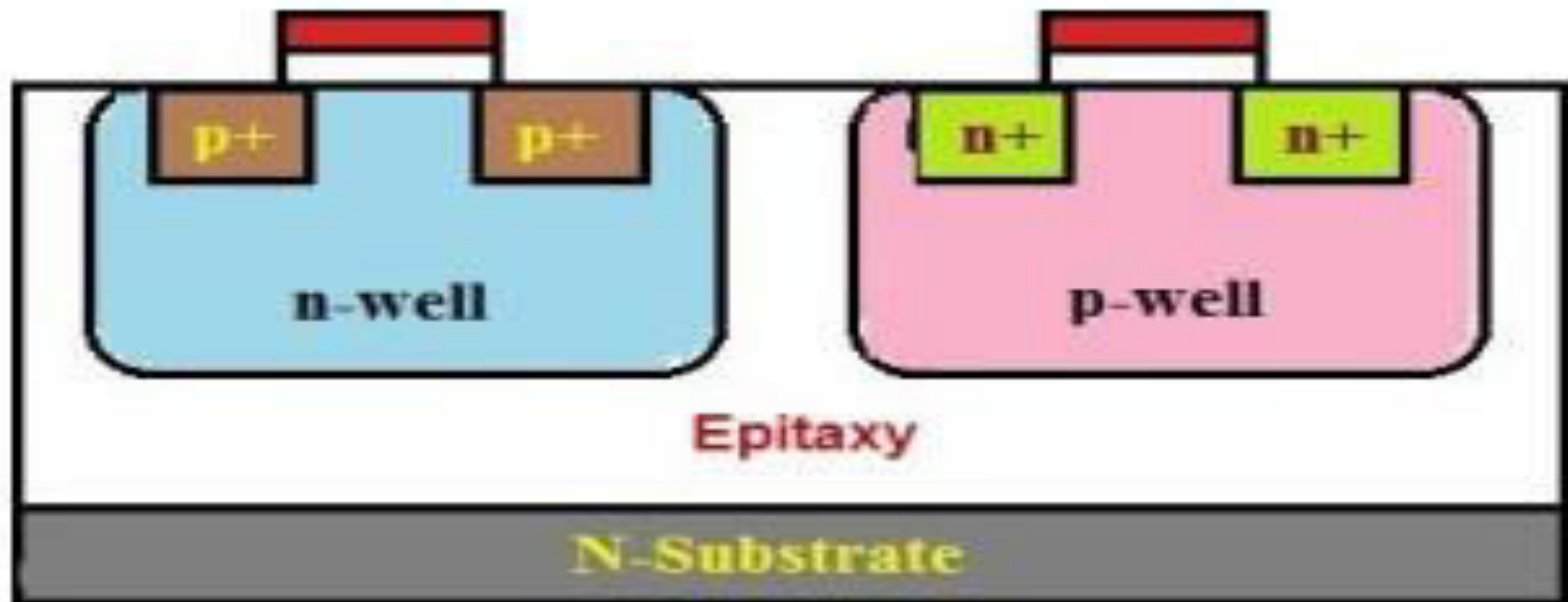
P well process video



<https://www.youtube.com/watch?v=oZAQMdHscSw> Prepared by Dr.Shylashree N

Twin Well Process

- ❑ In this process, separate optimization of the n-type and p-type transistors will be provided.
- ❑ The independent optimization of V_t , body effect and gain of the P-devices, N-devices can be made possible with this process.



Twin Well Process

Different steps of the fabrication of the CMOS using the twintub process are as follows:

- ❑ Lightly doped n⁺ or p⁺ substrate is taken and, to protect the latch up, epitaxial layer is used.
- ❑ An epitaxial layer is grown by depositing pure silicon on substrate. The epitaxial layer now acts like a substrate
- ❑ The high-purity controlled thickness of the layers of silicon are grown with exact dopant concentrations.
- ❑ The dopant and its concentration in Silicon are used to determine electrical properties.
- ❑ Formation of the tub
- ❑ Thin oxide construction
- ❑ Implantation of the source and drain
- ❑ Cuts for making contacts
- ❑ Metallization

Prepared by Dr.Shylashree N

By using the above steps we can fabricate CMOS using twintub process method.

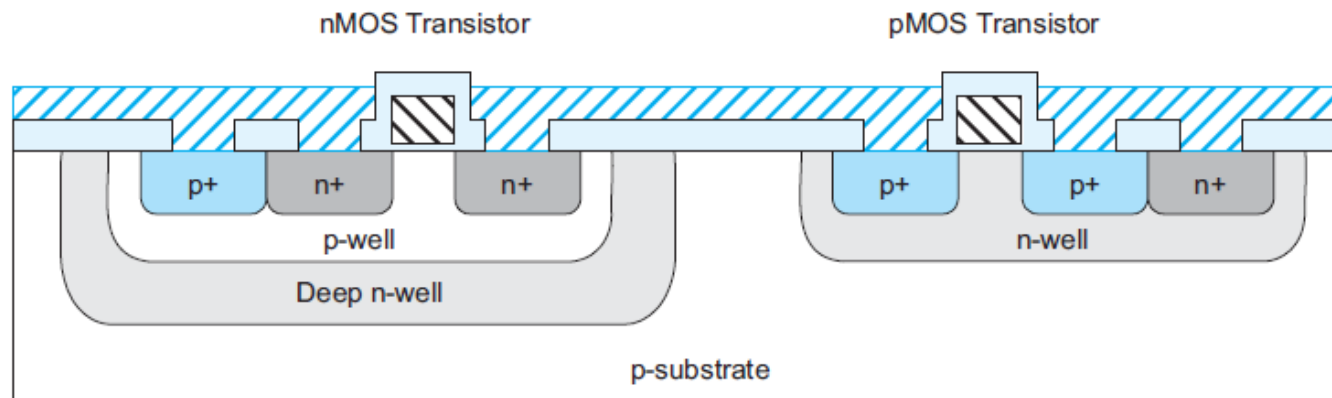
Twin Tub process video



<https://www.youtube.com/watch?v=gxpjHjSlvFc> Prepared by Dr.Shylashree N

Triple Well Process

- ❑ Noise injected into the substrate by digital circuits can disturb sensitive analog or memory circuits.
 - ❑ In a triple-well process, a deep n-well is first driven in to the p-type substrate, usually using high-energy (Mev-Mega electron volt levels) ion implantation as opposed to a thermally diffused operation
- Prepared by Dr.Shylashree N



CMOS Processing Technology

4. Well & Channel Formation

- ▣ Epitaxy: involves growing a single-crystal film on the silicon surface by subjecting the silicon wafer surface to an elevated temperature and a source of dopant material.

Epitaxy can be used to produce a layer of silicon with fewer defects than the native wafer surface and also can help prevent latchup.

Prepared by Dr.Shylashree N

Well & Channel Formation

- ❑ Deposition: Involves placing dopant material on to the silicon surface and then driving it in to the bulk using a thermal diffusion step. This can be used to build deep junctions. A step called CVD can be used for the deposition.

- ❑ Ion Implantation

Prepared by Dr.Shylashree N

- involves bombarding the silicon substrate with highly energized donor or acceptor atoms. When these atoms impinge on the silicon surface, they travel below the surface of the silicon, forming regions with varying doping concentrations.

Silicon dioxide – Oxidation

- Silicon dioxide has a number of uses in the IC fabrication process.
 - Silicon has dominated the industry because it has an easily processable oxide (i.e it can be grown and etched).
 - Various thickness of SiO_2 may be required, depending on the particular process.
 - Thin oxides are required for transistor gates: thicker oxide may be required for higher voltage devices. Used for device isolation
 - Used for gate oxide
 - Used as protecting buffer layer in device fabrication

Prepared by Dr.Shylashree N

Silicon dioxide – Oxidation

- Oxidation of silicon is achieved by heating silicon wafers in an oxidizing atmosphere.
- Wet oxidation: When the oxidizing atmosphere contains water vapor. The temperature is usually between 900°C and 1000°C . This is also called pyrogenic oxidation when a 2:1 mixture of hydrogen and oxygen is used. Wet oxidation is a rapid process.

Silicon dioxide – Oxidation

- Dry oxidation: When the oxidizing atmosphere is pure oxygen. Temperature are in the region of 1200°C to achieve an acceptable growth rate. Dry oxidation forms a better quality oxide than wet oxidation. It is used to form thin, highly controlled gate oxides, while wet oxidation may be used to form thick field oxides.

Prepared by Dr.Shylashree N

- Atomic layer deposition (ALD) – a process in which a thin chemical layer (material A) is attached to a surface and then a chemical (material B) is introduced to produce a thin layer of the required layer. The process is then repeated and the required layer is built up layer by layer.

Comparison of different oxidation approaches

Wet Oxidation	Dry Oxidation
Oxidizing atmosphere contains water vapor	Oxidizing atmosphere is pure oxygen
Temperature : 900 °C - 1000 °C	Temperature : 1200 °C
Low quality oxide	Better quality oxide
Form thick field oxides	Thin, highly controlled gate oxides

Atomic layer deposition : used for other dielectrics and metals

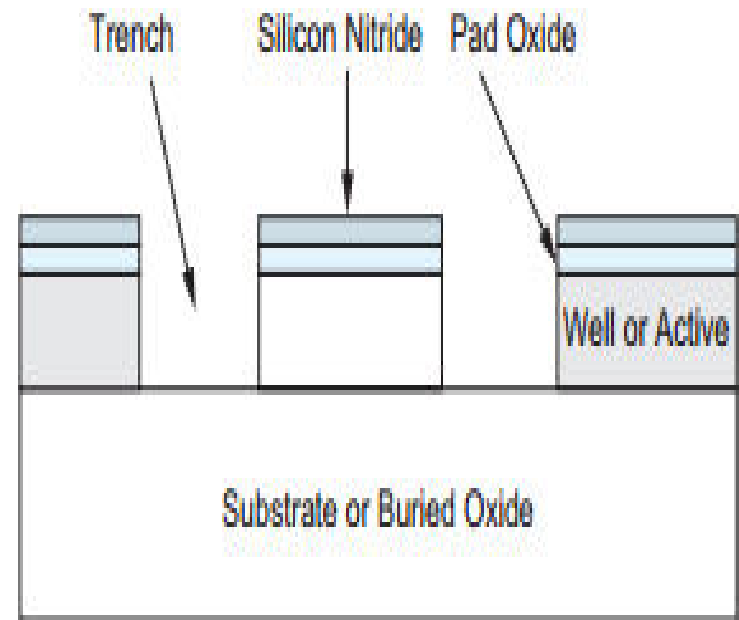
Prepared by Dr.Shylashree N

Isolation

- ❑ Individual devices in a CMOS process need to be isolated from one another so that they do not have unexpected interactions.
- ❑ The isolation step that is used to achieve isolation between in processes at and below the 180nm node is to form insulating trenches of SiO_2 that surround active areas.
- ❑ Typical trenches in a 90nm process can be 140nm wide by 400nm deep. This is called shallow trench isolation (STI)

Isolation contd..

- STI starts with a pad oxide and a silicon nitride layer, which act as the masking layers.
- Opening in the Pad oxide are then used to etch into the well or substrate region.

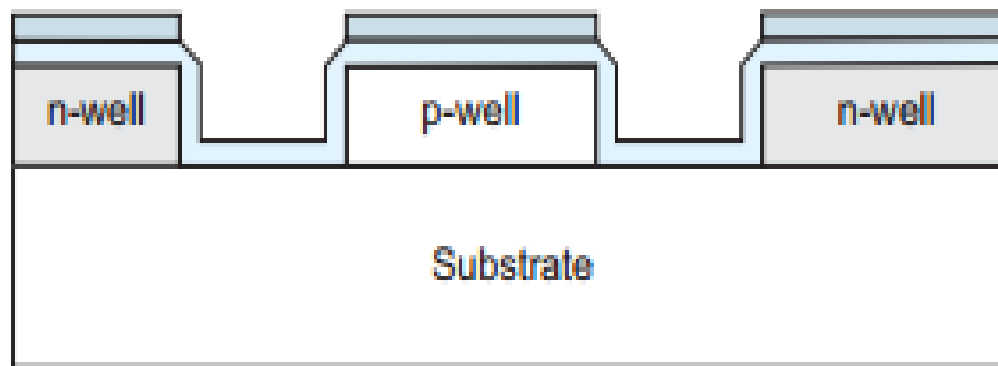


(a) Trench Etch

Isolation contd..

- A linear oxide is then grown to cover the exposed silicon.

Prepared by Dr.Shylashree N

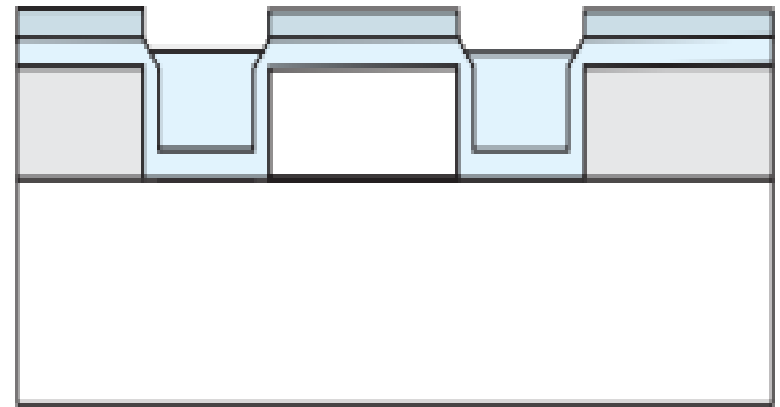


(b) Liner Oxidation

Isolation contd..

- The trenches are filled with SiO_2 using CVD that does not consume the underlying silicon.

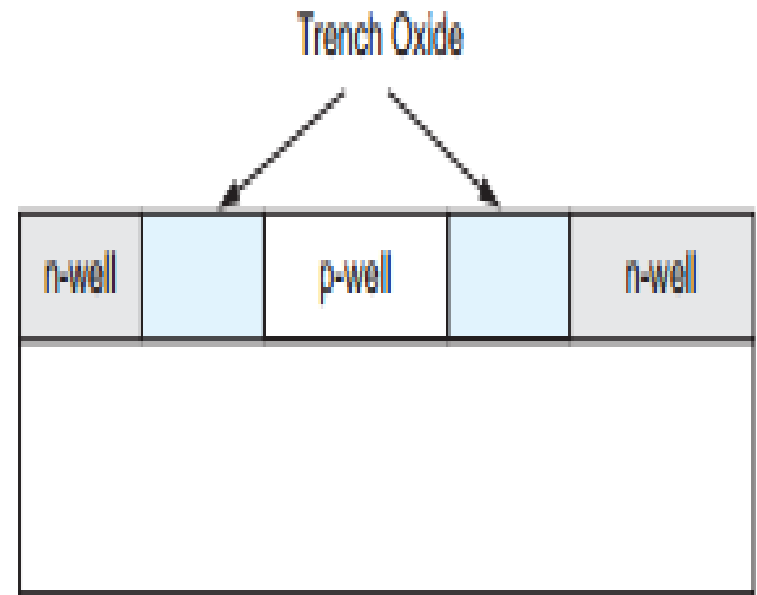
Prepared by Dr.Shylashree N



(c) Fill Trench with Dielectric

Isolation contd..

- The pad oxide and nitride are removed and a chemical mechanical polishing (CMP) step used to planarize the structure.



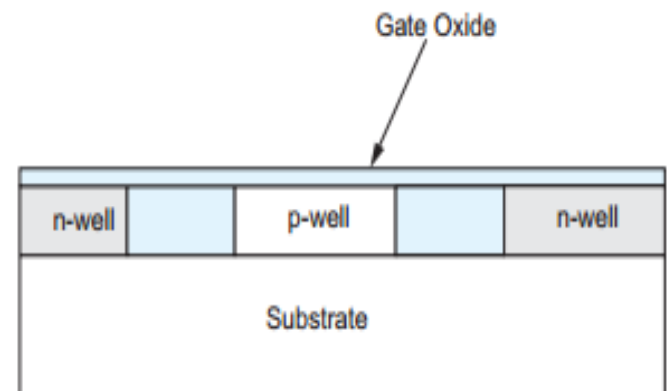
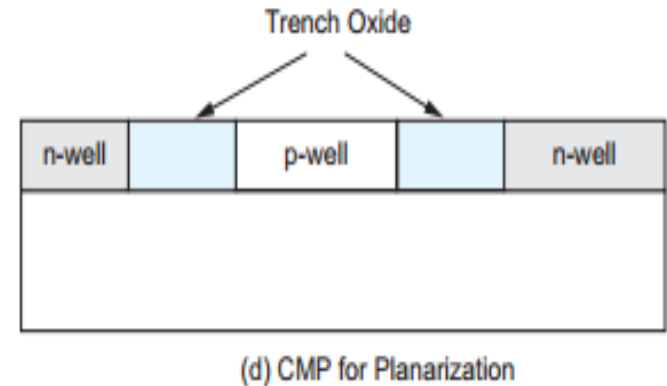
(d) CMP for Planarization

Isolation contd..

- CMP is used to achieve flat surfaces, which are of central importance in modern processes with many layers.
 - From the designers perspective, the presence of deep n-well and or trench isolation makes it easier to isolate noise sensitive portions of a chip from digital sections.
 - Trench isolation also permits nMOS and pMOS transistors to be placed closer together because the isolation provides a higher source/drain breakdown voltage.
- Prepared by Dr.Shylashree N
- The breakdown voltage must exceed the supply voltage and is determined by the junction dimensions and doping levels of the junctions formed

Gate Oxide

- In the case of STI-defined source/drain regions, that gate oxide is grown on top of the planarized structure that occurs at the stage shown in Fig. (a)
- This is shown in Fig.(b).The oxide structure is called the gate stack.



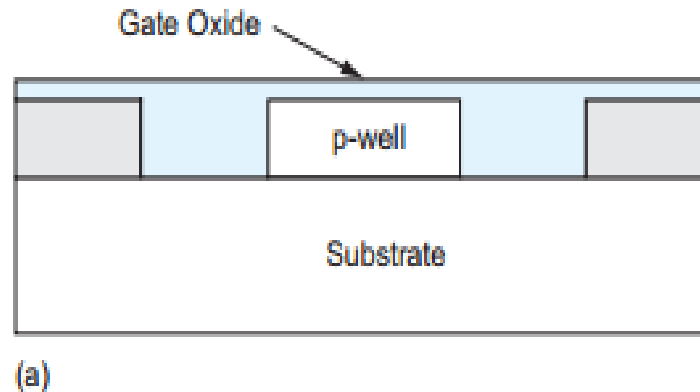
Gate Oxide

- The presence of the nitrogen increases the dielectric constant, which decreases the effective oxide thickness (EOT); this means that for a given oxide thickness, it performs like a thinner oxide.
- Being able to use a thicker oxide improves the robustness of the process.

Prepared by Dr.Shylashree N

Gate and Source/Drain Formation

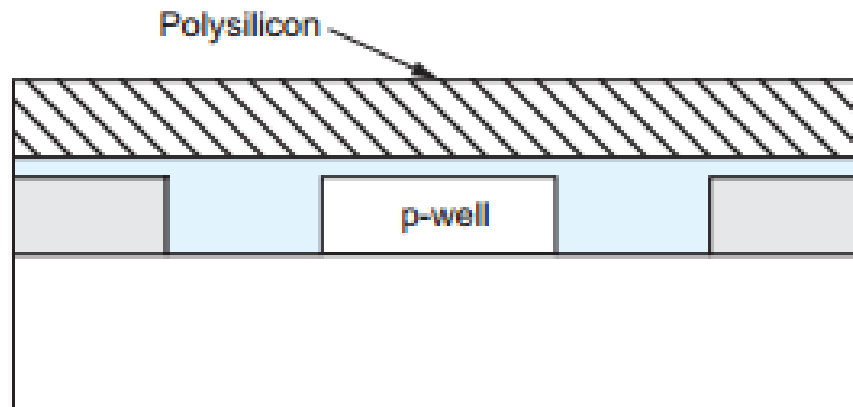
- ❑ The polysilicon gate serves as a mask to allow precise alignment of the source and drain with the gate. This process is called a self-aligned polysilicon gate process.
- ❑ The steps to define the gate, source, and drain in a self-aligned polysilicon gate are as follows:



(a). Grow gate oxide wherever transistors are required (area = Source+drain+gate) elsewhere there will be thick oxide

Gate and Source/Drain Formation

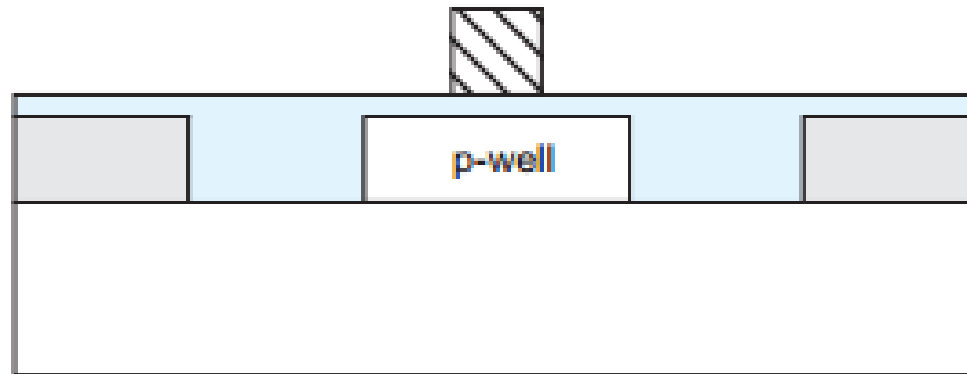
(b). Deposit polysilicon on chip



(b)

Gate and Source/Drain Formation

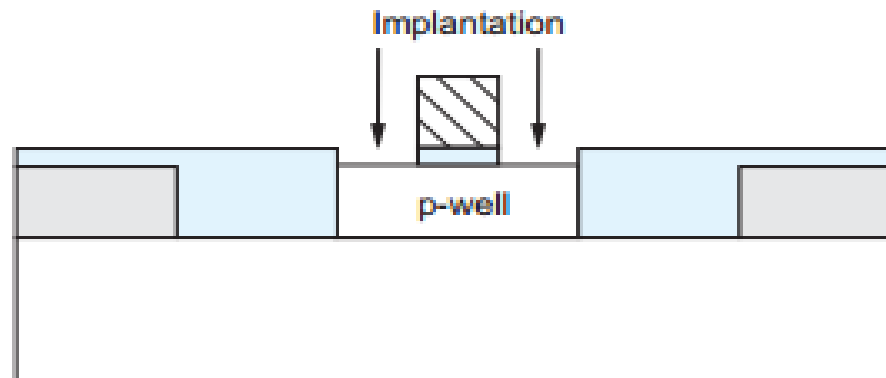
(c) Pattern polysilicon (both gates and interconnect)



(c)

Gate and Source/Drain Formation

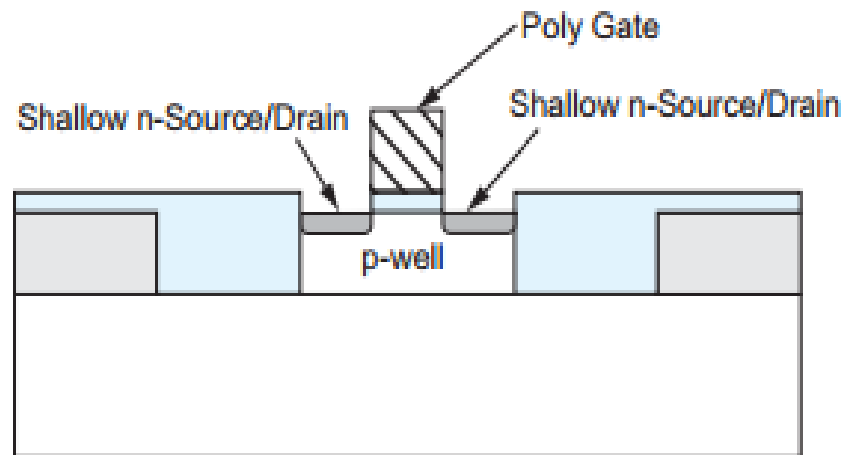
(d) Etch exposed gate oxide—that is, the area of gate oxide that was not covered by polysilicon; at this stage, the chip has windows down to the well or substrate wherever a source/drain diffusion is required.



(d)

Gate and Source/Drain Formation

(e) Implant pMOS and nMOS source/Drain regions

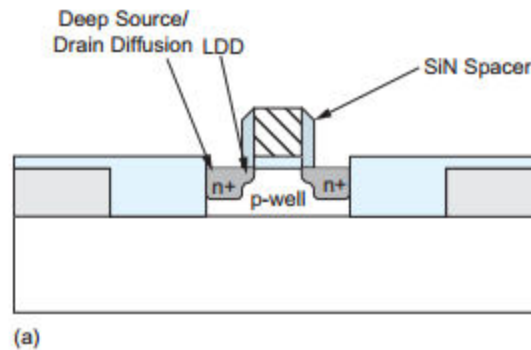


(e)

The source/drain implant is relatively low, typically in the range 10^{18} - 10^{20} cm^{-3} of impurity atoms. Such a lightly doped drain (LDD) structure reduces the electric field at the drain junction, which improves the immunity of the device to hot electron damage.

Lightly Doped Drain (LDD) Structure

LDD implants are shallow and lightly doped, so they exhibit low capacitance but high resistance. This reduces device performance somewhat because of the resistance in series with the transistor.



Consequently, deeper, more heavily doped source/drain implants are needed to provide devices that combine hot electron suppression with low source/drain resistance. A silicon nitride (Si_3N_4) spacer along the edge of the gate serves as a mask to define the location of this deeper diffusion as shown in Fig(a).

Lightly Doped Drain (LDD) Structure

A layer of silicide is formed when the two substances react at elevated temperatures. In a polycide process, only the gate polysilicon is silicided. In a silicide process both gate polysilicon and source/drain regions are silicided. This process lowers the resistance of the polysilicon interconnect and/or the source and drain.

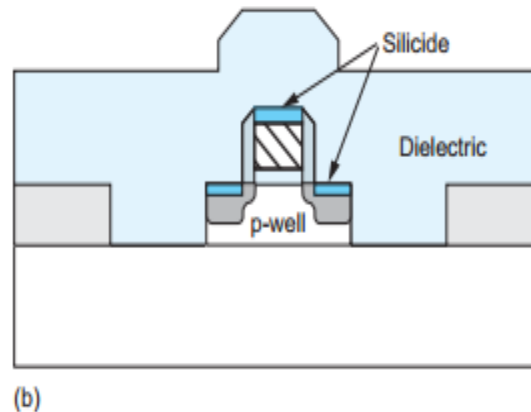
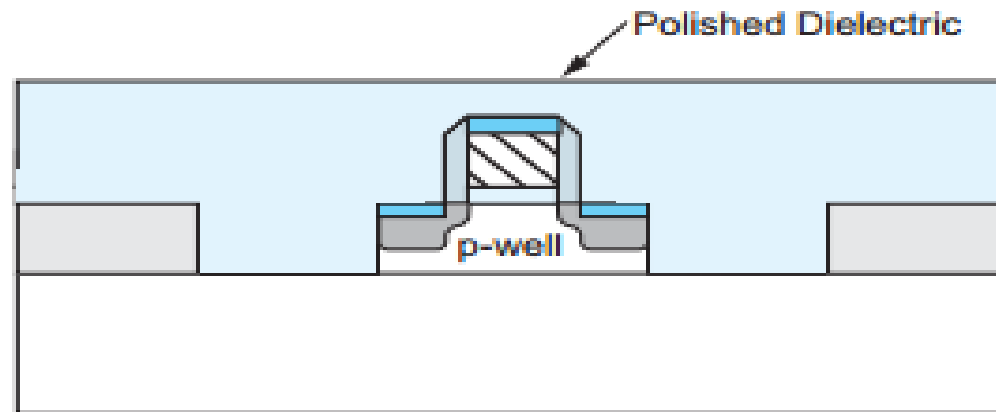


Fig.(b) shows the resultant structure with gate and source/drain regions silicided. In addition, SiO_2 or an alternative dielectric has been used to cover all areas prior to the next processing steps.

Lightly Doped Drain (LDD) Structure

Fig (c) shows a structure where CMP has been employed. Achieving a very flat finish allows layers to be stacked vertically without incurring the problems of metal

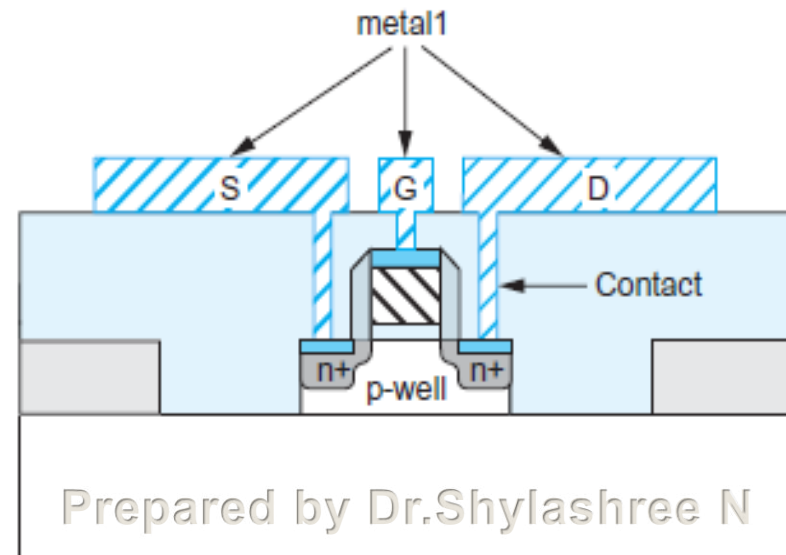


(c)

Contacts & Metallization

- Contact cuts are made to source, drain, and gate according to the contact mask.
- Metallization is the process of building wires to connect the devices
 - ▣ Evaporation – Performed by passing a high electrical current through a thick Al wire in a vacuum chamber, Al atoms are vaporized and deposited on the wafer.
 - ▣ Sputtering - Performed by generating a gas plasma by ionizing an inert gas using an RF or DC electric field. The ions are focused on Al target and the plasma dislodges metal atoms, which are then deposited on the wafer.

- Wet or dry etching can be used to remove unwanted metal.
- Plasma etching is a dry etch process with chlorine gas used for metallization steps.



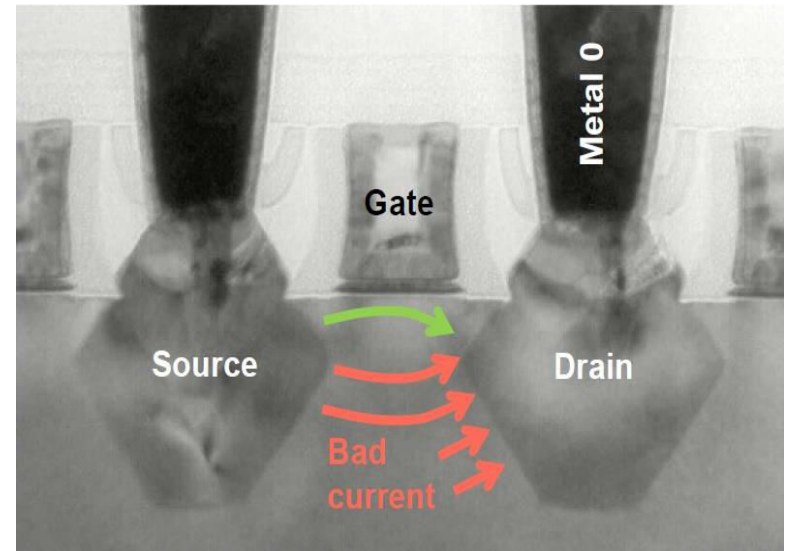
Passivation

- ❑ The final processing step is to add a protective glass layer called passivation or overglass.
- ❑ This prevents the ingress of contaminants.
- ❑ Openings in the passivation layer, called overglass cuts, allow connection to I/O pads and test probe points.

Prepared by Dr.Shylashree N

Metrology

- ❑ Metrology is the science of measuring
- ❑ Measurement of everything built in a semiconductor process to give feedback to the manufacturing process
- ❑ Optical microscopes are used to observe large structures and defects
- ❑ Scanning Electron Microscopy – SEM used to observe very small wavelength of visible light $\sim 0.5\mu\text{m}$.
- ❑ Transmission Electron Microscope – TEM which observes the results of passing electrons through a sample, is sometimes also used to measure structures.



Lambda(λ) Design Rules

- λ based design rules makes the design dimension in terms of λ . This is independent of the technology used. The technology adopted will decide suitable value for λ .

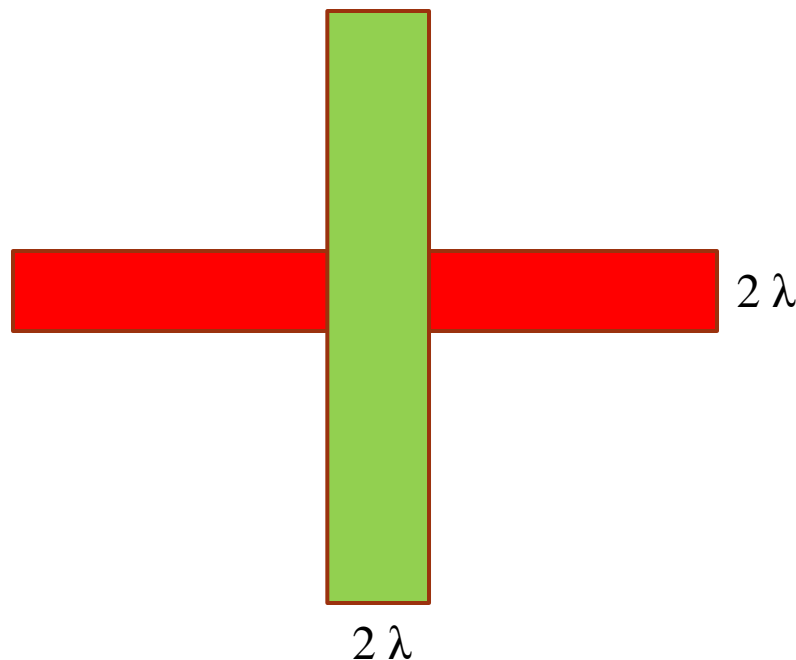
- Minimum width of layers/wires

1.	n-diffusion - 2λ		2λ
2.	p-diffusion - 2λ		2λ
3.	Polysilicon - 2λ		2λ
4.	Metal 1 - 3λ		3λ
5.	Metal 2 - 4λ		4λ

Lambda(λ) Design Rules contd..

□ Transistor Dimensions

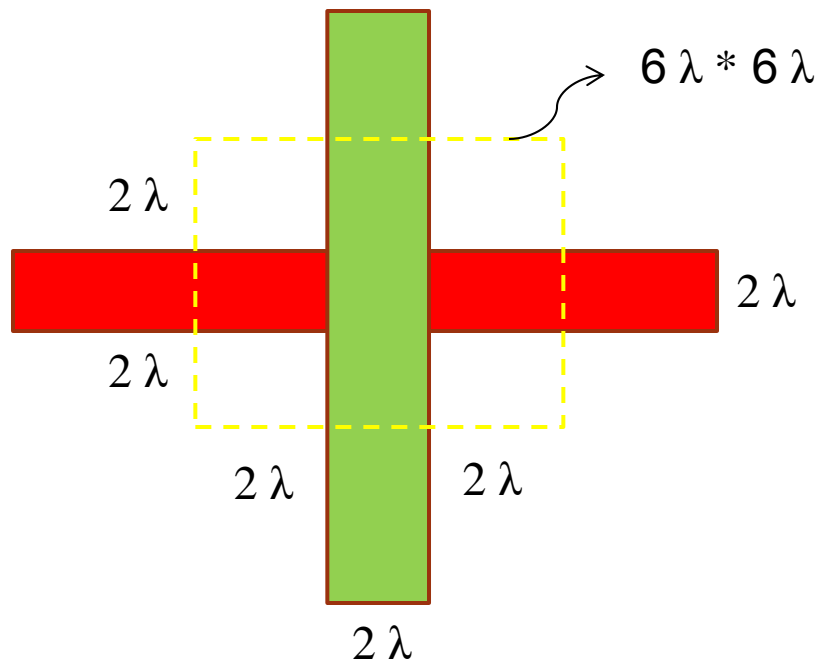
1. Minimum dimension = $2\lambda * 2\lambda$



Transistor being overlap of polysilicon and diffusion, the minimum dimension of each layer being 2λ and the transistor is a square of $2\lambda * 2\lambda$

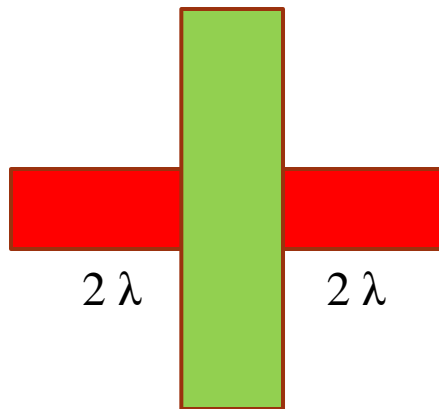
Lambda(λ) Design Rules contd..

2. Implant: The implant should extend by 2λ from both polysilicon and diffusion.



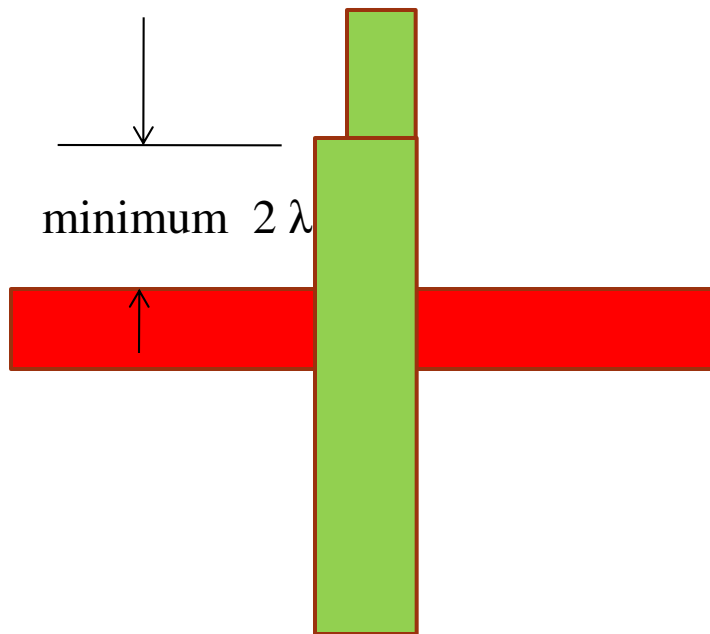
Lambda(λ) Design Rules contd..

3. Polysilicon should extend diffusion by at least 2λ



Lambda(λ) Design Rules contd..

4. The width of the diffusion should not change within a distance of 2λ from the boundary of polysilicon

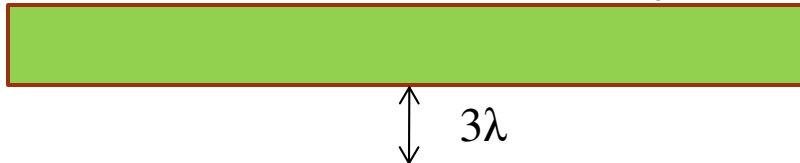


Lambda(λ) Design Rules contd..

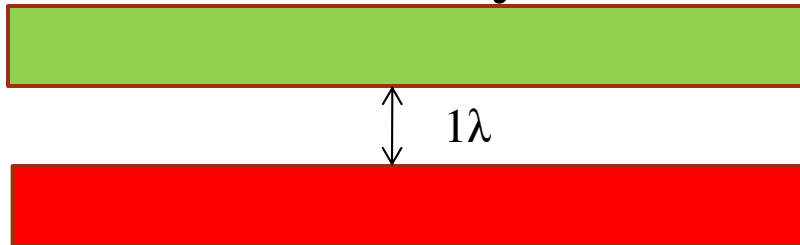
□ Spacing or separation rules

The minimum distance between various wires are as follows.

1. Diffusion – Diffusion (Thin oxide region) = 3λ

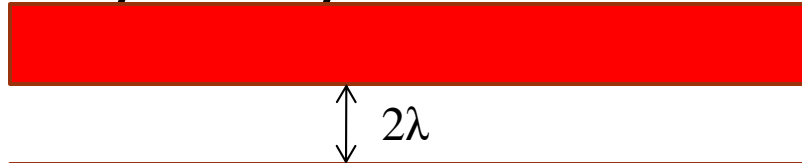


2. Diffusion to Poly = 1λ

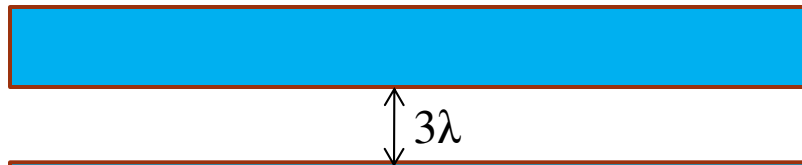


Lambda(λ) Design Rules contd..

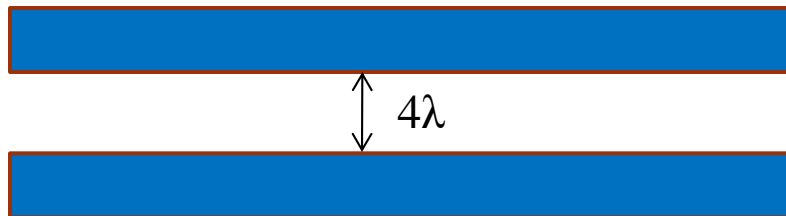
3. Poly – Poly = 2λ



4. Metal 1 to Metal 1 = 3λ



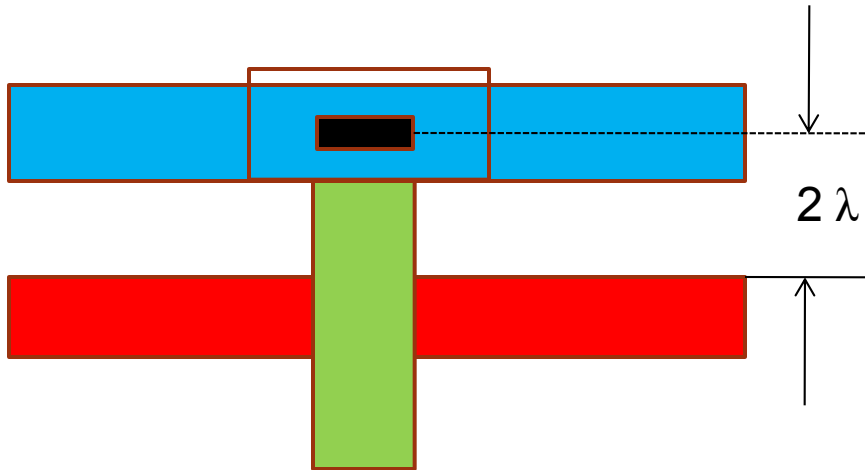
5. Metal 2 to Metal 2 = 4λ



Between any 2 layers if the separation rule is not specified, then those layers can cross i.e, metal can cross both polysilicon and diffusion.

Lambda(λ) Design Rules contd..

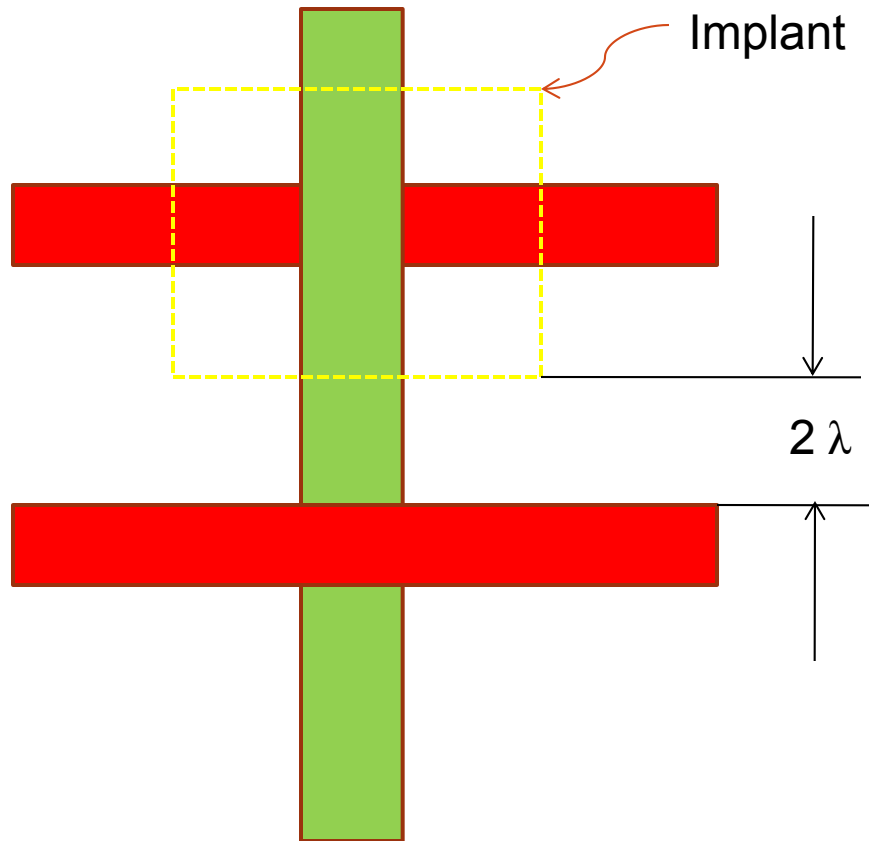
6. Minimum distance between Metal contact and transistor = 2λ



Prepared by Dr.Shylashree N

Lambda(λ) Design Rules contd..

7. Implant and next transistor = 2λ

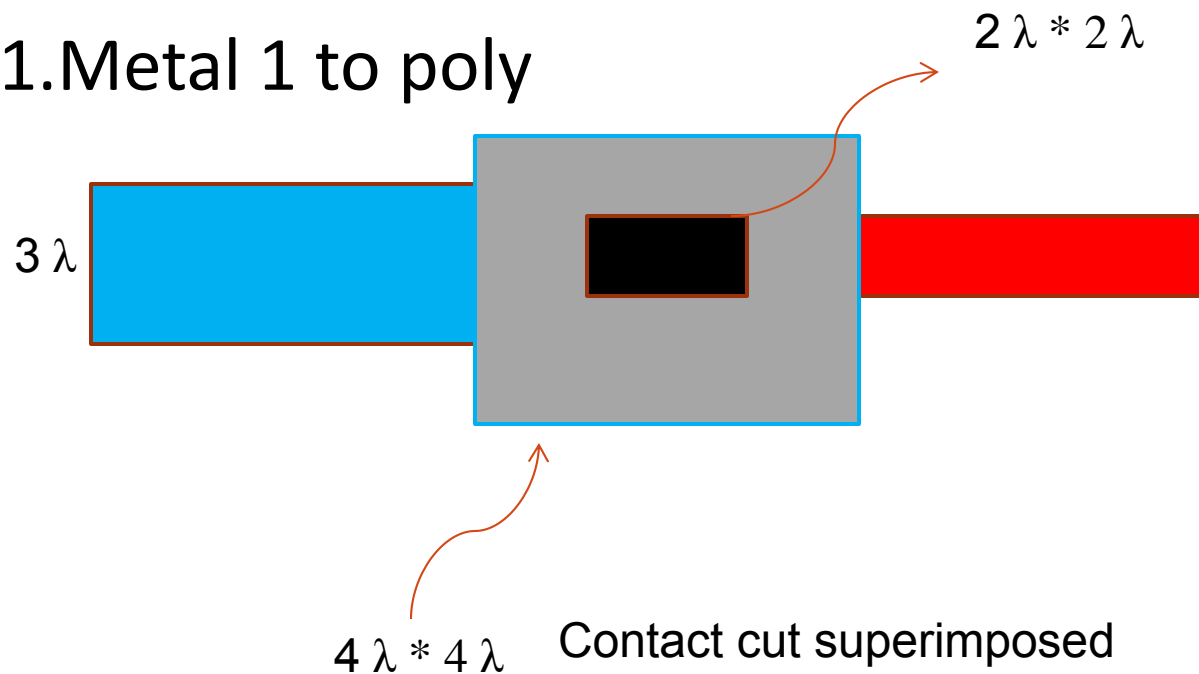


Prepared by Dr.Shylashree N

Lambda(λ) Design Rules contd..

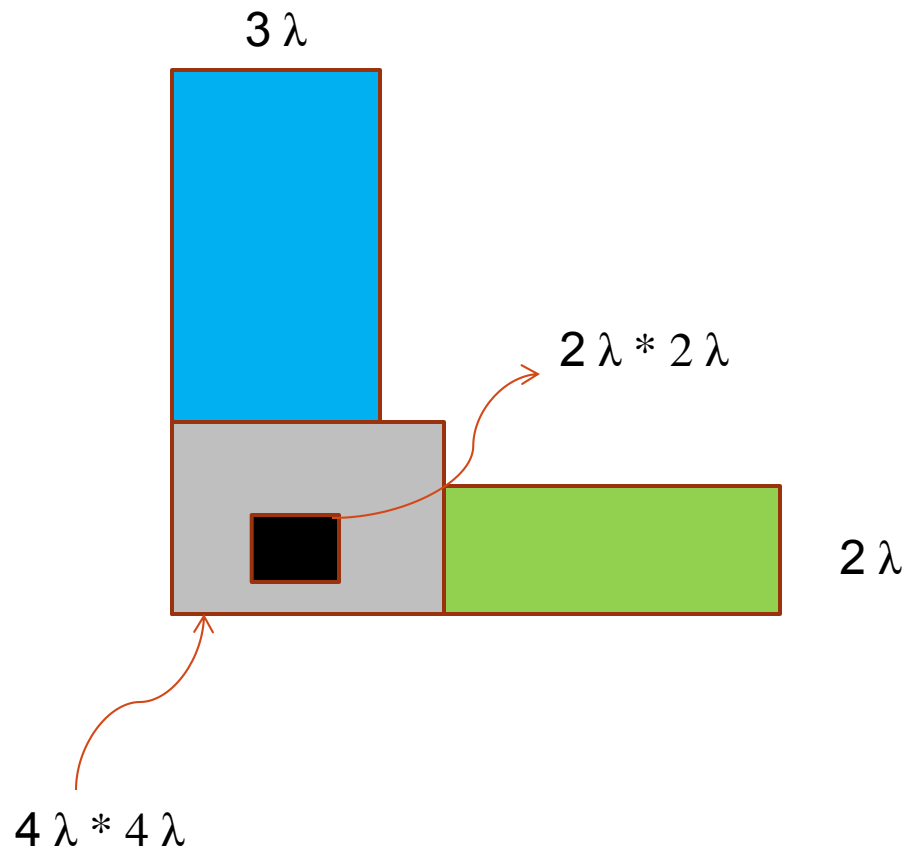
□ Design rules for contacts

1. Metal 1 to poly



Lambda(λ) Design Rules contd..

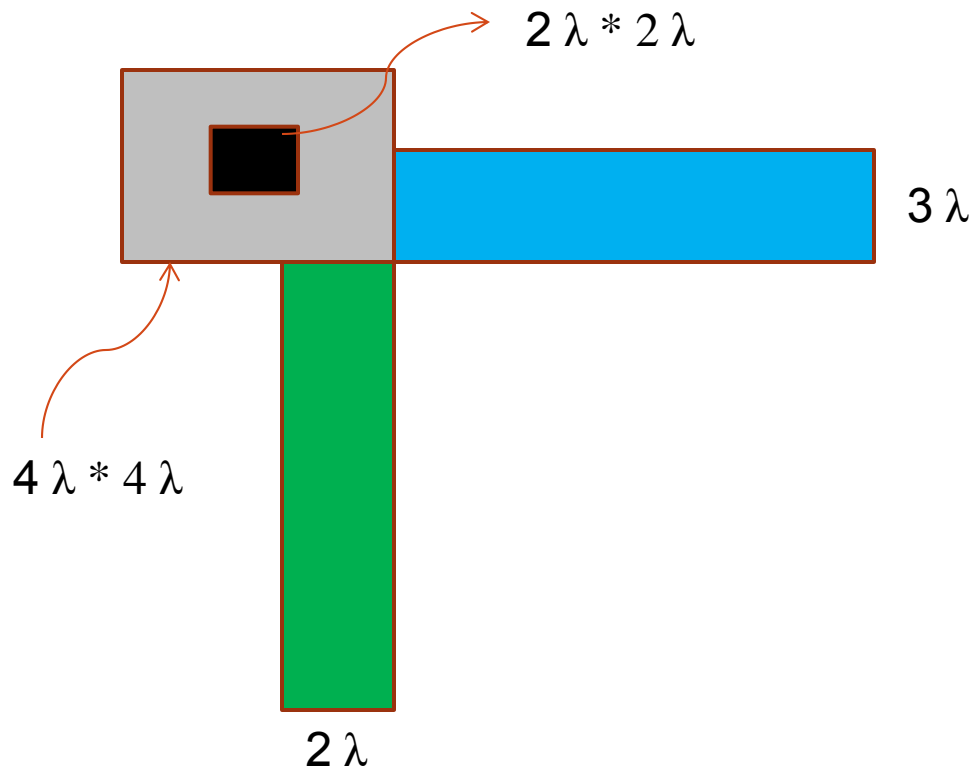
2. Metal 1 – n diffusion



Prepared by Dr.Shylashree N

Lambda(λ) Design Rules contd..

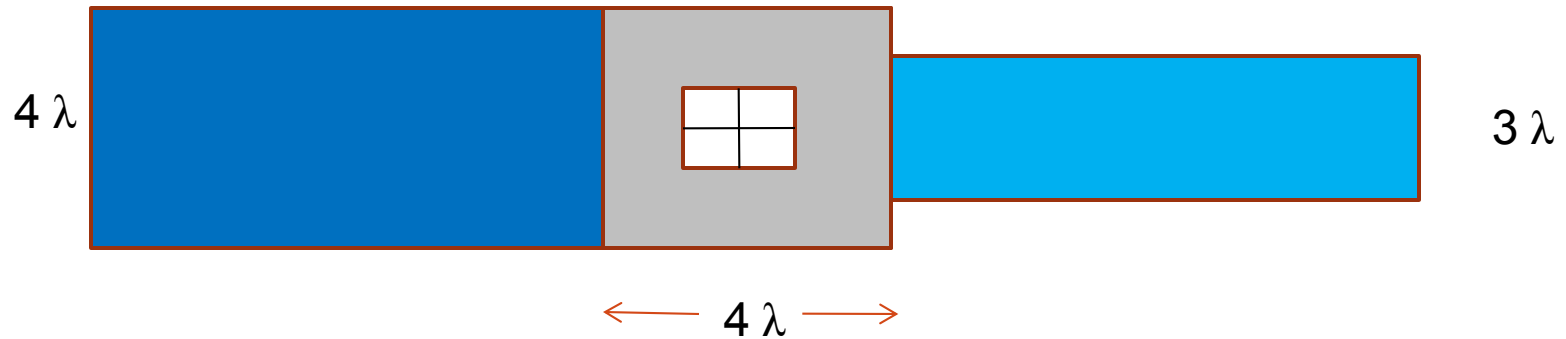
3.P-diffusion – Metal 1



Prepared by Dr.Shylashree N

Lambda(λ) Design Rules contd..

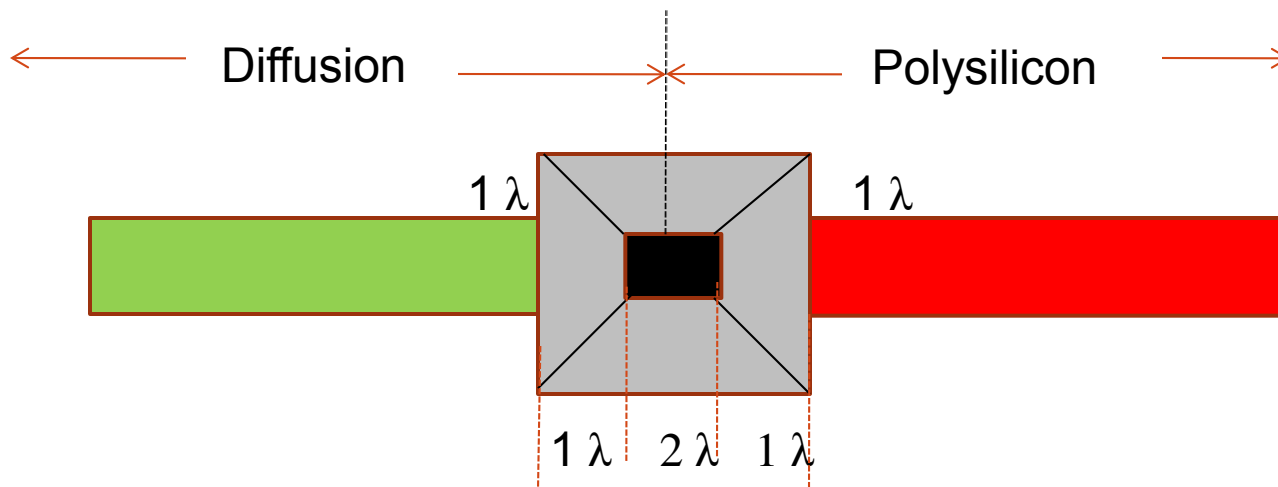
4. Metal 2 – Metal 1



Prepared by Dr.Shylashree N

Lambda(λ) Design Rules contd..

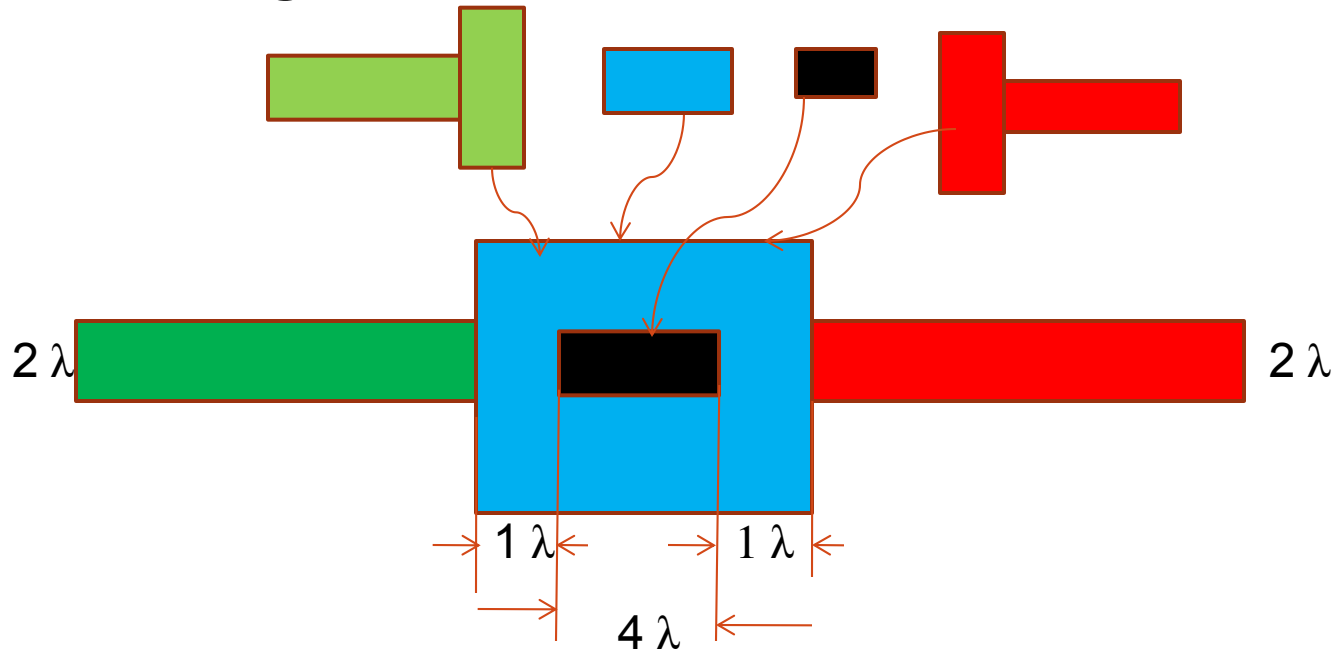
5. Buried Contact



The buried contact is made with $2\lambda * 2\lambda$ contact at centre and the layers extending beyond the cut area at least by 1λ in all directions.

Lambda(λ) Design Rules contd..

6. Butting contact



A butting contact is established when polysilicon layer is connected to diffusion layer through metal.

Lambda(λ) Design Rules contd..

□ Butting contact contd...

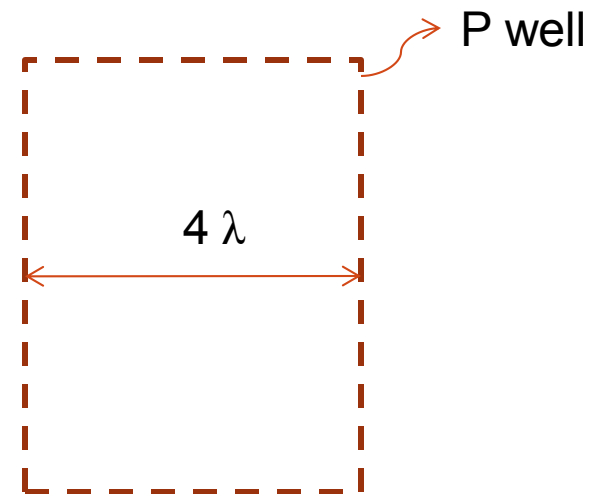
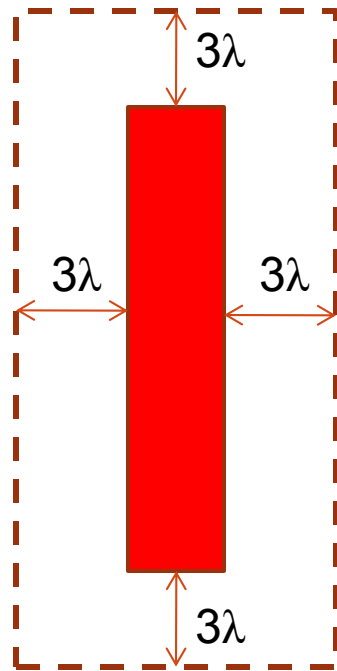
$2\lambda * 2\lambda$ cut is made both to diffusion and polysilicon. Hence contact cut becomes $4\lambda * 2\lambda$ and is continuous. Metal extends beyond contact cut by 1λ in all directions.

λ based rules as applied to CMOS circuits

- All λ based rules of MOS circuits are applicable with the following additional rules.

Lambda(λ) Design Rules contd..

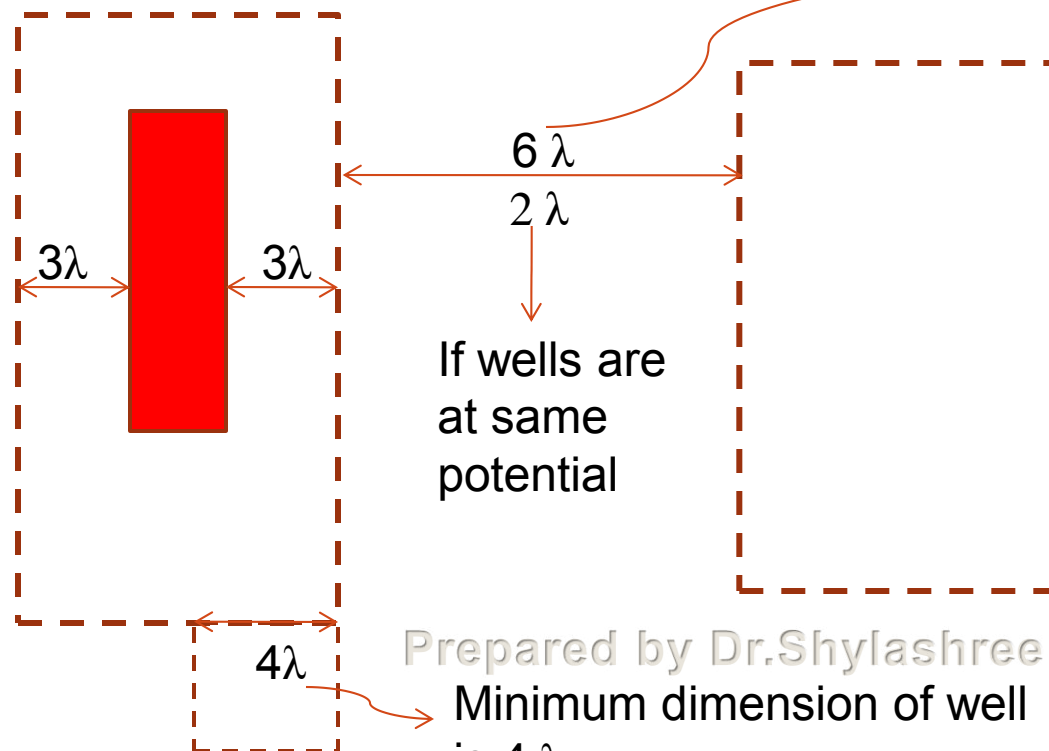
1. The P well must enclose diffusion and polysilicon within 3λ extension



Minimum dimension of well is 4λ

Lambda(λ) Design Rules contd..

2. The distance of separation between 2 p-wells should be 2λ if wells are at same potential and 6λ if wells are at different potential.

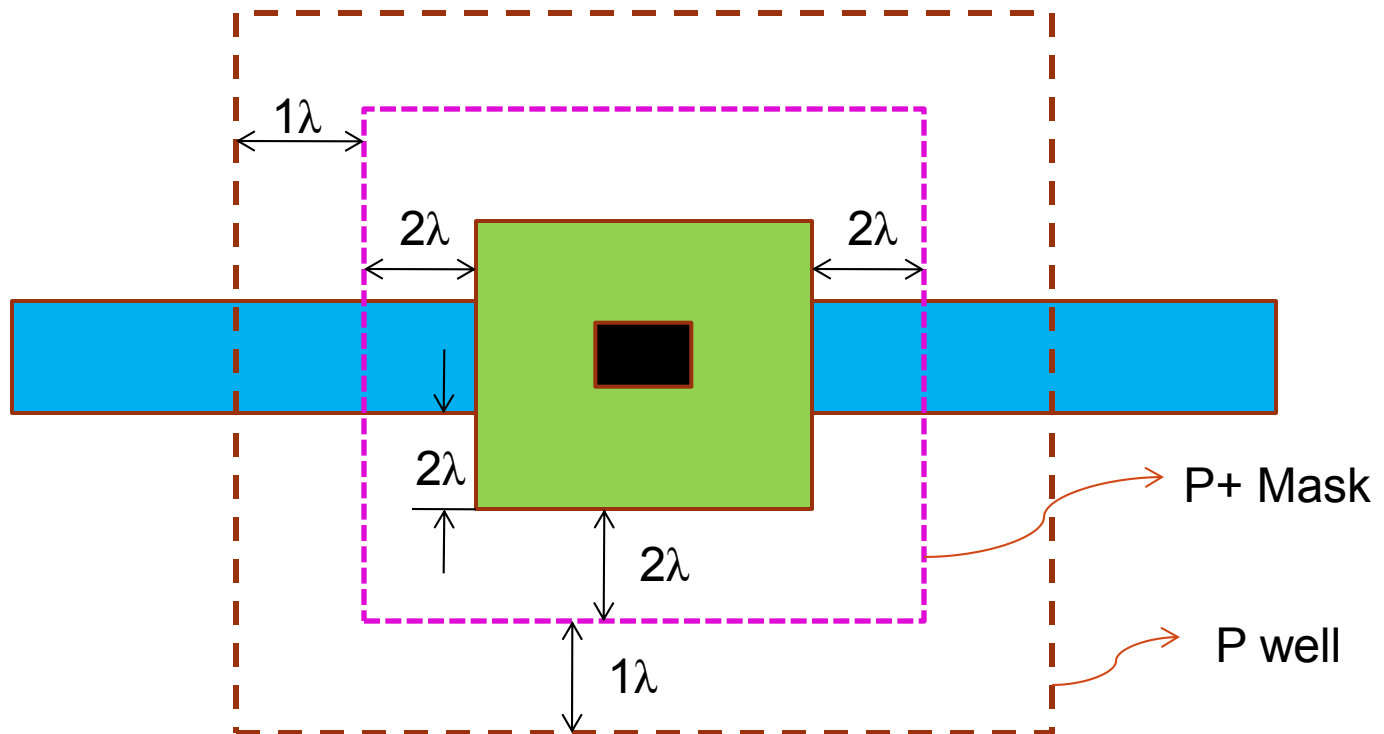


Prepared by Dr.Shylashree N

Minimum dimension of well
is 4λ

Lambda(λ) Design Rules contd..

3. The well contact has to be enclosed within a P⁺ mask

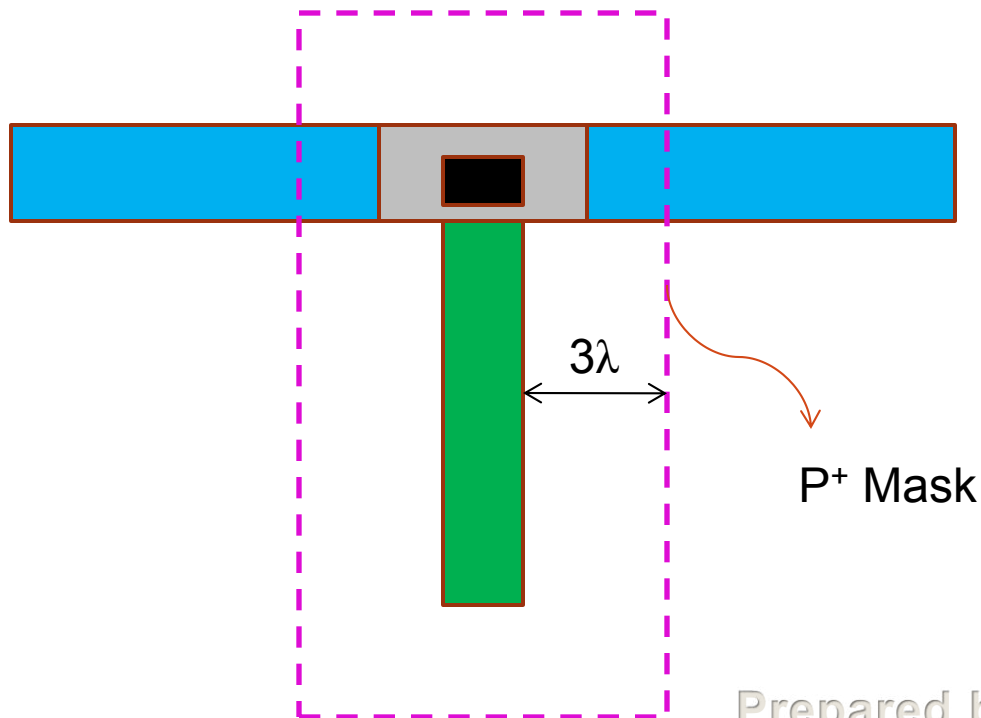


Prepared by Dr.Shylashree N

Extending 2λ from the contact in all direction. The distance of separation between P⁺ mask and well is 1λ .

Lambda(λ) Design Rules contd..

4. All P-diffusions in the substrate must be enclosed by a P⁺ mask and mask must extend P diffusion by 3λ



Introduction to MOSFET scaling

- The process of reducing vertical and horizontal dimensions of MOSFETs is called scaling.
- Scaling is defined as the process of reducing the horizontal and vertical dimension of a MOS device by some scaling factor S , which is greater than 1.
- This, the scaled device is obtained by simply dividing the key dimension of the MOSFET, such as channel length (L), channel width (W), oxide thickness (t_{ox}) and junction depth (X_j), by a scaling factor S .

Transistor Scaling contd..

- Two types of schemes commonly used for MOSFET scaling are constant voltage scaling and constant field scaling. (More details - Micro electronics by Shedra Smith)

Scaling factors for device Parameters.

1. Gate Area A_g

$$A_g = L W$$

Where L & W are the channel length and width respectively. Both are scaled by $1/\alpha$. Thus A_g is scaled by $1/\alpha^2$

Transistor Scaling contd..

2. Gate capacitance per unit area C_o or C_{ox}

$$C_o = \epsilon_{ox} / D$$

Where ϵ_{ox} is the permittivity of the gate oxide (thinox) and D is the gate oxide thickness which is scaled by $1/\beta$.

Thus C_o is scaled by $1 / (1/ \beta) = \beta$

3. Gate capacitance C_g

$$C_g = C_o \cdot L \cdot W$$

Prepared by Dr.Shylashree N

Thus C_g is scaled by $\beta \cdot 1/ \alpha^2 = \beta/ \alpha^2$

Transistor Scaling contd..

4. Parasitic Capacitance C_x

C_x is proportional to A_x/d .

Where 'd' is the depletion width around source or drain which is scaled by $1/\alpha$, and A_x is the area of the depletion region around source or drain which is scaled by $1/\alpha^2$.

Thus is C_x scaled by $1/\alpha^2 \cdot 1/(1/\alpha) = 1/\alpha$.

5. Carrier density in channel Q_{on}

$$Q_{on} = C_O \cdot V_{gs}$$

Prepared by Dr.Shylashree N

Where Q_{on} is the average charge pr unit area in the

Transistor Scaling contd..

Channel in the 'on' state. Note that C_0 is scaled by β and V_{gs} is scaled by $1/\beta$.

Thus Q_{on} is scaled by 1.

6. Channel resistance R_{on}

$$R_{on} = L/W \cdot 1/Q_{on}\mu$$

Where μ is the carrier mobility in the channel and is assumed constant.

Thus R_{on} is scaled by $1/\alpha \cdot 1/(1/\alpha) \cdot 1 = 1$

Transistor Scaling contd..

7. Gate delay T_d

T_d is proportional to $R_{on} \cdot C_g$

Thus T_d is scaled by $1/\beta/\alpha^2 \cdot \beta/\alpha^2$

8. Maximum operating frequency f_O

$$f_O = W/L \cdot \mu C_O V_{DD} / C_g$$

or f_O is the inversely proportional to delay T_d

Thus, f_O is scaled by $1/(\beta/\alpha^2) = \alpha^2 / \beta$

9. Saturation current I_{dss}

$$I_{dss} = C_O \mu / 2 \cdot W/L \cdot (V_{gs} - V_t)^2$$

Transistor Scaling contd..

Noting that both V_{gs} and V_t are scaled by $1/\beta$, we have I_{dss} is scaled by $\beta(1/\beta)^2 = 1/\beta$.

10. Current Density J

$$J = I_{dss}/A$$

Where A is the cross sectional area of the channel in the 'on' state which is scaled by $1/\alpha^2$.

So, J is scaled by $(1/\beta)/(1/\alpha^2) = \alpha^2/\beta$

11. Switching energy per gate E_g

$$E_g = 1/2 C_g (V_{DD})^2$$

Prepared by Dr.Shylashree N

So, E_g is scaled by $\beta/\alpha^2 \cdot 1/\beta^2 = 1/\alpha^2 \beta$

Transistor Scaling contd..

12. Power dissipation per gate P_g

P_g comprises two components such that

$$P_g = P_{gs} + P_{gd}$$

Where the static component

$$P_{gs} = (V_{DD})^2 / R_{on}$$

and the dynamic component

$$P_{gd} = E_g f_O$$

It will be seen that both P_{gs} and P_{gd} are scaled by $1/\beta^2$.

So, P_g is scaled by $1/\beta^2$

Transistor Scaling contd..

13. Power dissipation per unit area P_a

$$P_a = P_g / A_g$$

So, P_a is scaled by $(1/\beta^2)/(1/\alpha^2) = \alpha^2/\beta^2$

14. Power speed product P_T

$$P_T = P_g \cdot T_d$$

So, P_T is scaled by $1/\beta^2 \cdot \beta/\alpha^2 = 1/\alpha^2\beta$

References

1. Neil H.E.weste, david harris, Ayan Banerjee, “CMOS VLSi Design”, Pearson education, 3rd Edition, 2006, ISBN:0321149017
2. Douglas A. Pucknell, Kamaran Eshraghian, “Basic VLSI Design”, PHI, 3rd edition 2010, ISBN:0-321-26977-2

Possible Questions

1. Explain the wafer formation using Czochralski method.
2. Explain photolithography process with suitable setup. Also explain how wavelengths of the light sources cause distortions in the pattern.
3. Briefly explain the different methods of metallization in IC fabrication.
4. Explain CMOS N-well fabrication process with the help of neat sketches and show the mask view for the same.

Possible Questions contd..

5. Describe with neat diagrams, the P-well fabrication process.
6. Explain with diagrams, the main steps in the twin-tub process.
7. With a neat sketch, explain shallow trench isolation.
8. With a neat sketch, explain LDD structure.
9. What is λ - based design? What are the merits and demerits?
10. With neat diagram, explain λ -based design rules for contact cuts and Vias.

Possible Questions contd..

11. Write the lambda based design rules for CMOS wires, transistors and contacts.
12. What is the need of scaling? Obtain scaling factor for maximum operating frequency using combined voltage and dimension scaling model.
13. Compute the scaling factors for the following device parameters in combined voltage and dimension scaling model.
 - i) Saturation current I_{dss}
 - ii) Gate capacitance
 - iii) Gate delay



Thank You